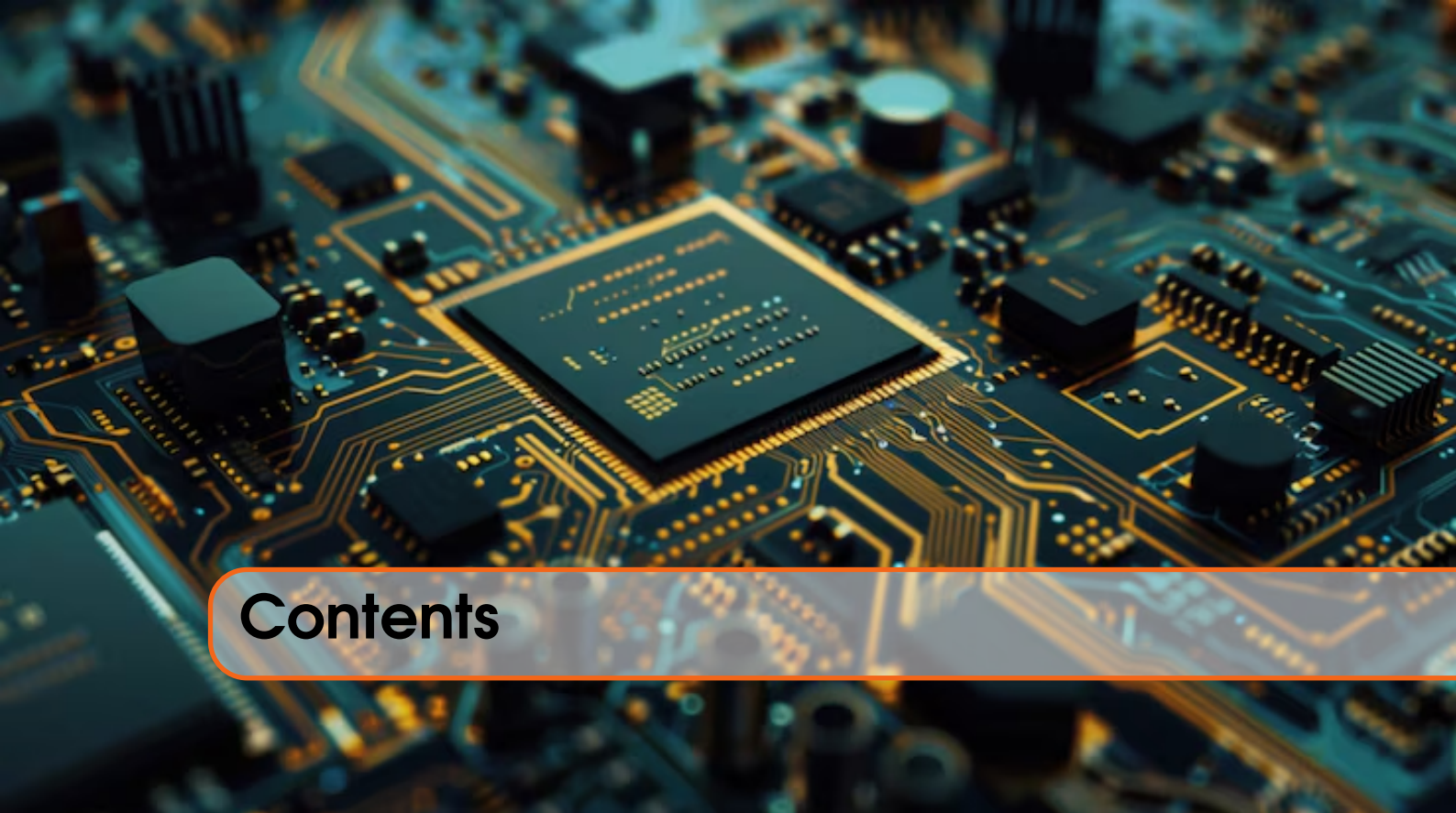


Analog VLSI Interview Questions

A Practical Question Set for Students

Satya Sai Kommana

FIRST EDITION



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About the Book

This book is a carefully collected set of real interview questions from Analog VLSI job interviews. These questions are based on the actual experiences of students from different IITs and NITs, who were interviewed by various semiconductor companies.

The main goal of this book is to help students build confidence. By solving many different types of questions on the same topic, students can learn to look at a concept from different angles. This helps develop a deeper and stronger understanding — which is very important for success in Analog VLSI interviews.

No new or artificial questions have been added by the author, as the intention is to give students a clear understanding of actual interview scenarios. Every question included is relevant and highlights key concepts that are essential for Analog VLSI engineers.

About the Author

Satya Sai Kommana completed his M.Tech from **IIT Kharagpur** with a specialization in Instrumentation and Integrated Electronics, Department of Electrical Engineering. He was the **topper of the specialization (2023–2025)** and is currently working as an **Analog Design Engineer at a reputed company**.

I would like to express my sincere gratitude to everyone who generously shared their valuable experience and contributed to this work. My heartfelt thanks also go to those who supported me and helped make this possible.

If you have any suggestions, would like to contribute to this material, or if you find any mistakes, please feel free to get in touch.

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About the Second and Third Editions

In the **Second Edition**, we plan to include:

- Detailed solutions for all questions
- Additional questions collected from fresh interview experiences
- Improved formatting and layout for better readability

Due to time constraints during the first edition, diagrams were not drawn for all questions and were directly pasted from the source. The main focus of this edition was on collecting questions.

In the **Third Edition**, we aim to make the learning experience even more interactive by:

- Providing recorded video solutions and embedding clickable links next to each solution that redirect to the specific video for that solution.

This feature is designed to make learning more intuitive, efficient, and student-friendly.

First release August 2025



Passive Circuits

1	First and Second Order Circuits . . .	6
1.1	Prerequisites	
1.2	RC Circuits	
1.3	RL Circuits	
1.4	RLC Circuits	

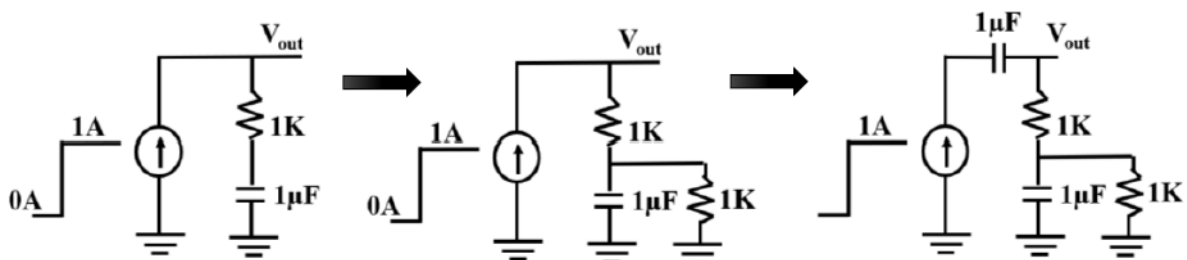
1. First and Second Order Circuits

1.1 Prerequisites

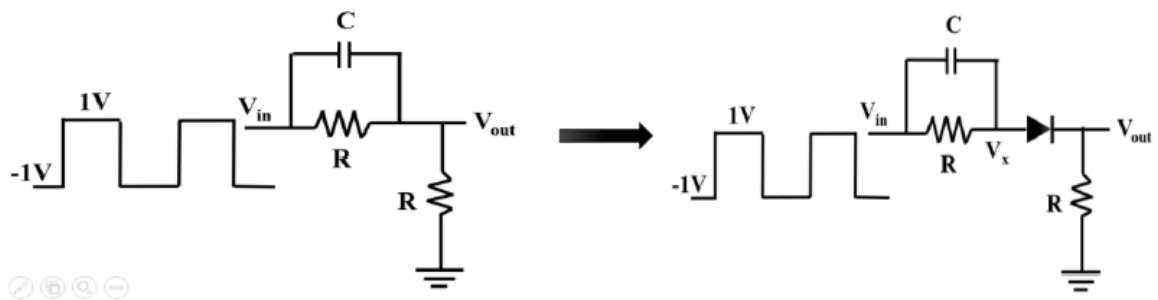
1. Introduction to Electrical Sciences (Passive Devices) - ES by Chembiyan T.
2. Basics of Signals for Transient Analysis by Himanshu Agarwal.
3. Prep For Interview || RC-RL-RLC-LC by Himanshu Agarwal.
4. Interesting Analysis on the Order of a Circuit || Prep for Interview by Himanshu Agarwal.
5. Transient Response of ALL RL Circuits With Current Source || VLSI Placements Interview Questions by Anish Saha.

1.2 RC Circuits

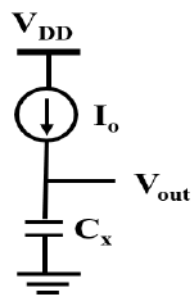
1. Find the time constant and draw V_{out} for all three cases.



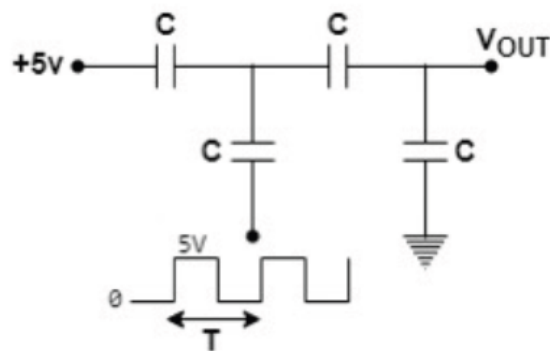
2.
 - a) Find the transfer function by inspecting the circuit.
 - b) Explain intuitively why the zero is located at $-\frac{1}{RC}$.
 - c) Draw V_{out} for the case when $\frac{T}{2} \gg \tau$, where $\tau = RC$ is the time constant.
 - d) Draw V_x and V_{out} after a diode is added, for $\frac{T}{2} \gg \tau$.



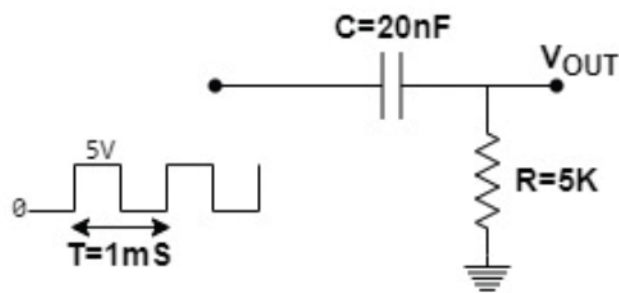
3. Is it possible for the output voltage V_{out} to exceed the supply voltage V_{DD} in practical scenarios? If so, under what conditions, and how is it achieved?



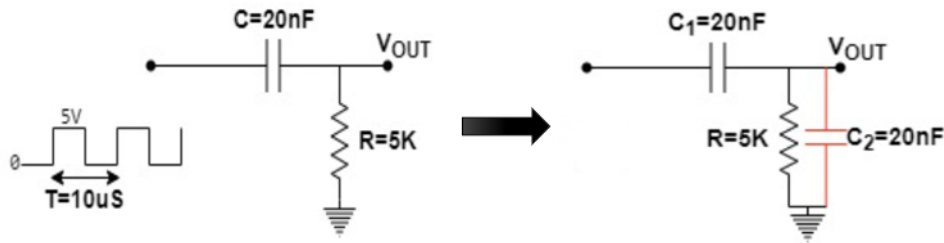
4. Draw V_{out} intuitively.



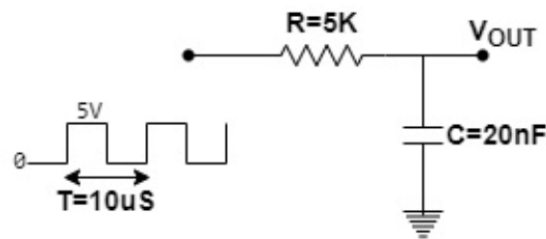
5. Draw V_{out} intuitively.



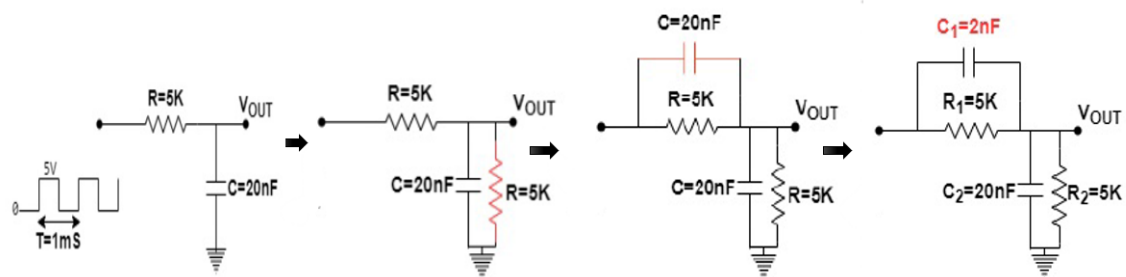
6. Draw V_{out} and follow up question was why is it trying to settle towards $V_{dd}/2$. Draw V_{out} after adding C_2 .



7. Draw V_{out} intuitively.



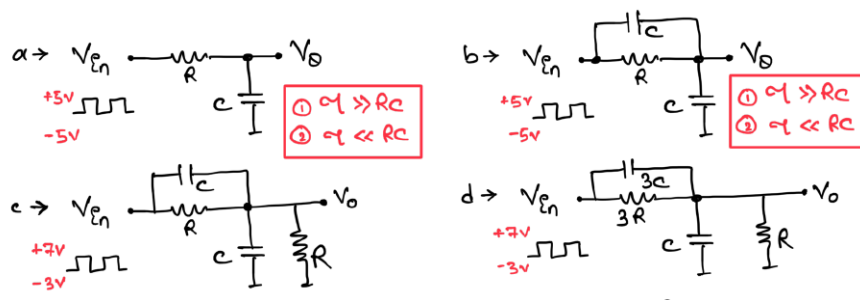
8. Draw V_{out} for all four cases and observe the differences between the outputs.



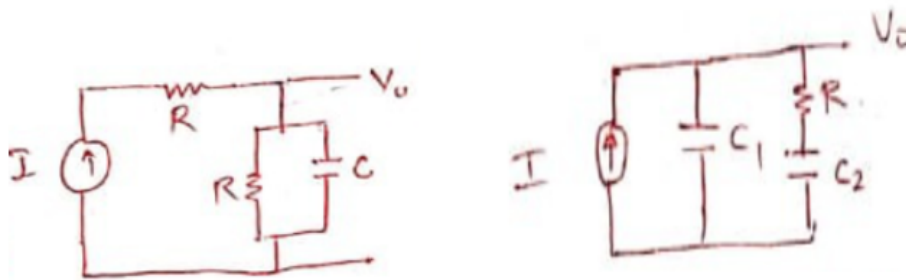
9. Draw V_{out} for all four figures with the following input types: (a) DC input and (b) square pulse input, under the following conditions:

(i) $RC \gg \tau$, (ii) $RC \ll \tau$, (iii) $RC = \tau$.

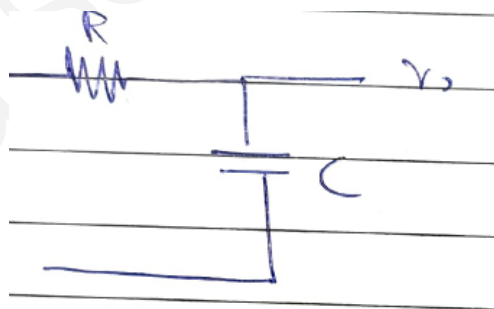
Observe the differences between the outputs.



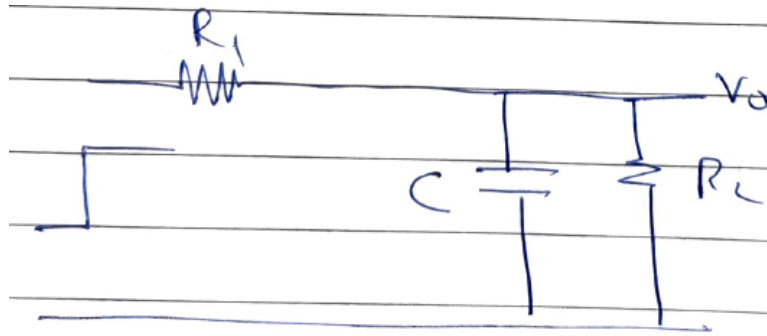
10. Find poles and zeros and draw bode plot.



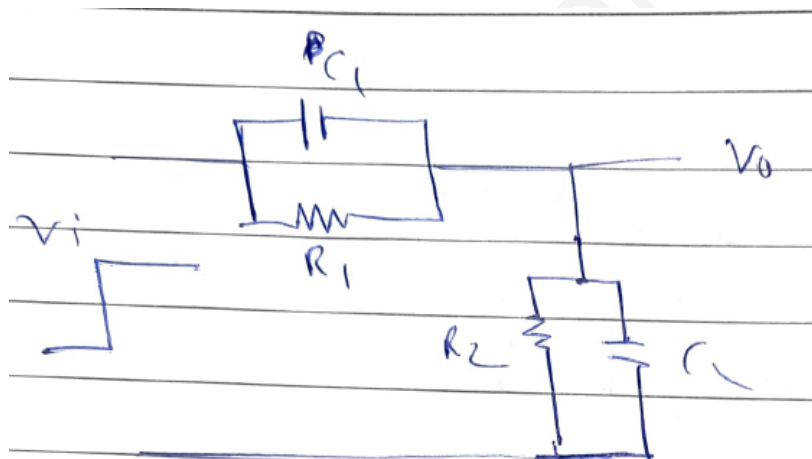
11. (a) Find the time constant τ of the given circuit.
 (b) Plot V_o for a step input. Explain intuitively what would happen by observing the circuit, without using any mathematics.
 (c) Change the input from a step input to a pulse input, and plot V_o for the following conditions: (i) $RC \gg \tau$, (ii) $RC \ll \tau$, (iii) $RC = \tau$.
 (d) Plot V_o for Impulse and ramp input.



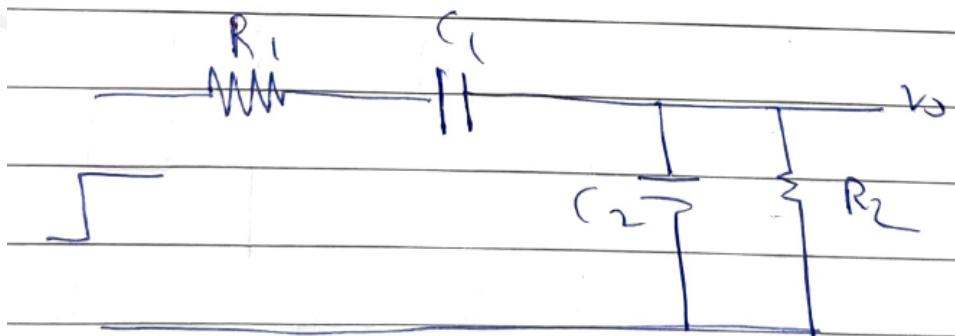
12. (a) Find the output voltage $V_o(t)$ for the given circuit. Explain intuitively what would happen by observing the circuit, without using any mathematics.
 (b) Determine the time constant τ of the circuit.
 (c) Intuitively analyze the poles and zeros of the circuit.
 (d) Find the transfer function of the circuit intuitively.
 (e) Draw the Bode plot.
 (f) If we substitute $s = -\frac{1}{\tau}$ (where τ is the time constant of the circuit), it appears that the transfer function becomes infinite. Why is this not reflected in the Bode plot?
 (g) What element can be added to the existing circuit to make the response obtained in Case (a) faster or to eliminate the delay in reaching steady state?



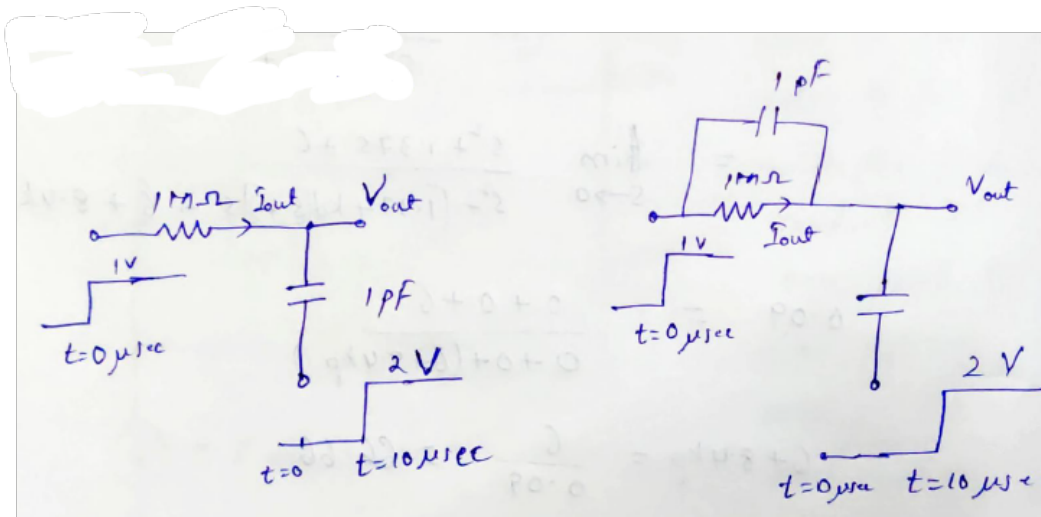
13. (a) Find the output voltage V_o for the following cases: (i) $R_1 C_1 > R_2 C_2$, (ii) $R_1 C_1 < R_2 C_2$, (iii) $R_1 C_1 = R_2 C_2$.
 (b) Explain why the voltage V_o jumps at the beginning of the input.
 (c) Determine the order of the system and explain.
 (d) What is the 3 dB bandwidth of the circuit?
 (e) The response obtained in (a) for the case $R_1 C_1 = R_2 C_2$ shows no delay or zero rise time. Then, what does the time constant in (d) represent?



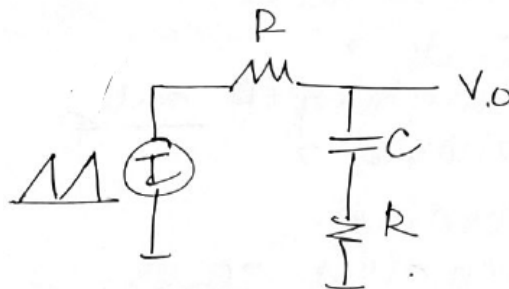
14. (a) Find the poles and zeroes of the system.
 (b) Determine the order of the system.
 (c) Find the output voltage $V_o(t)$.
 (d) Determine whether $V_o(\infty) = V_i$ is possible or not.



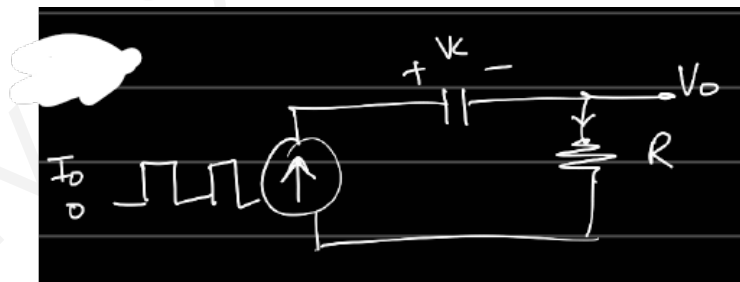
15. Draw the waveforms of V_{out} and I_{out} , and clearly mark important points on the plots.



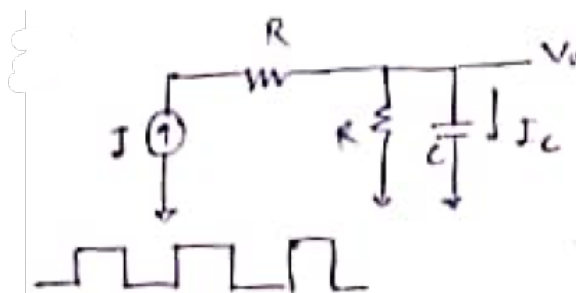
16. For a sawtooth current input I_{in} , what will be the output voltage V_o waveform?



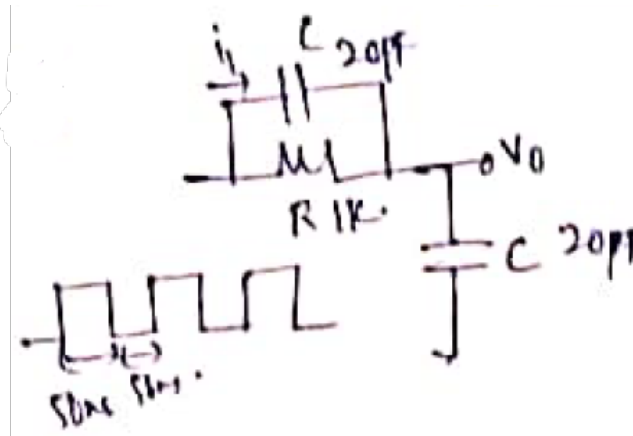
17. The capacitor is precharged to V_{co} . Plot V_o , V_c .



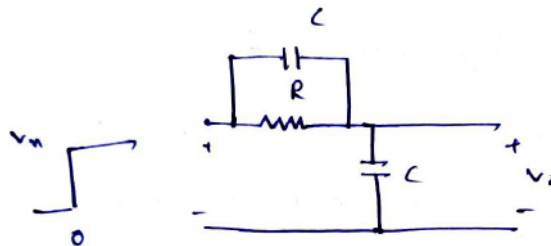
18. Plot V_o , I_c .



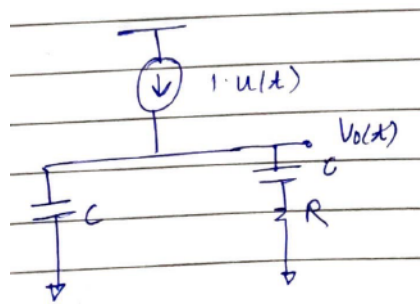
19. A pulse input with a period of 100 ns has an on-time and off-time of 50 ns. The value of $R = 1 \text{ k}\Omega$ and all capacitors $C = 20 \text{ pF}$.
- Draw i_1 and V_o .
 - Find the discharge rate of the capacitor C that is in parallel with R .



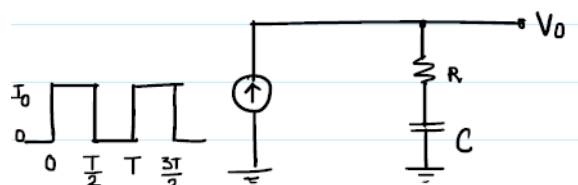
20. Find the poles and zeros of the circuit. Plot V_o for step and impulse inputs. Explain intuitively what would happen by observing the circuit, without using any mathematics.



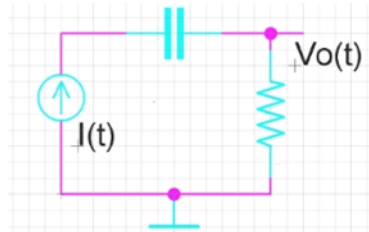
21. Steady-state response of V_o .



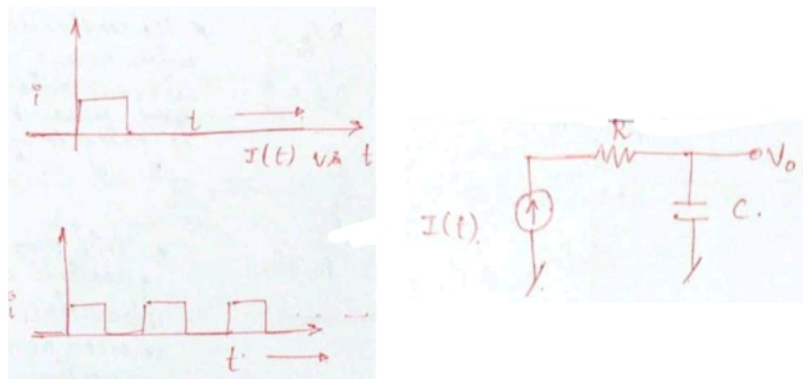
22. Plot V_o



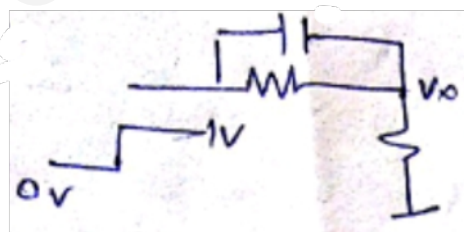
23. Explain the significance of poles and zeros in any system, and how to find them. What is their effect on the behavior of systems or circuits?
24. Draw $V_o(t)$ for $t > 0$ given that $I(t) = u(t)$.



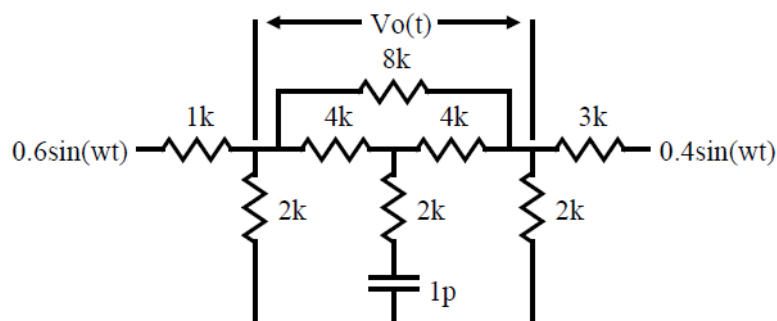
25. Plot V_o for the two types of $I(t)$ shown below. These types of questions are conventionally dealt with by writing voltage and current equations in the time domain, but an interviewer may also ask you to establish the relationship in the frequency domain using the Laplace transform.



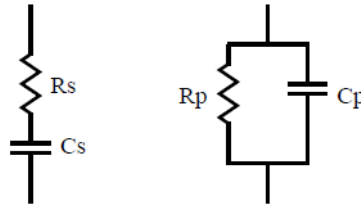
26. Plot V_x . Plot the current through both resistors. Explain intuitively what would happen by observing the circuit, without using any mathematics. Also find the time constant.



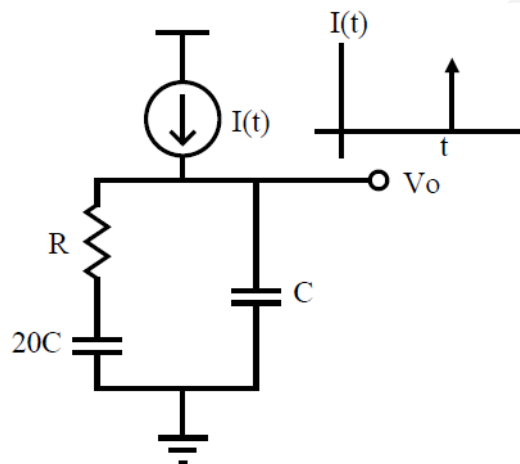
27. Determine the output voltage $V_o(t)$ for the circuit shown below.



28. The two circuits are equivalent. Express R_p and C_p in terms of R_s and C_s . Determine the frequency range ω for which the two circuits are equivalent, assuming a high quality factor (Q).

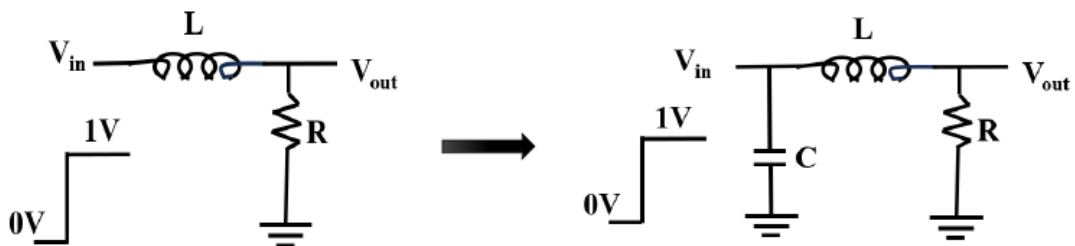


29. Plot the output voltage V_{out} as a function of time based on the given circuit conditions.

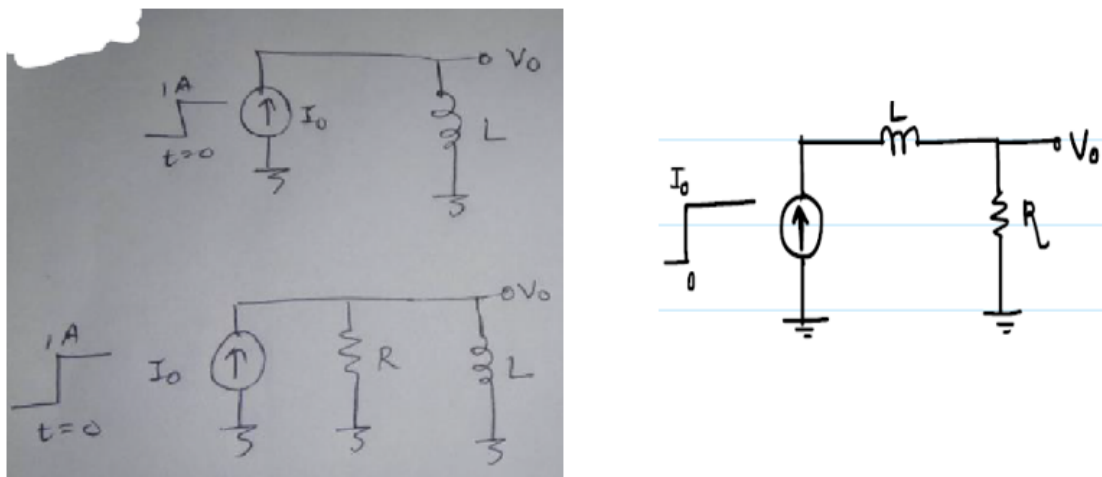


1.3 RL Circuits

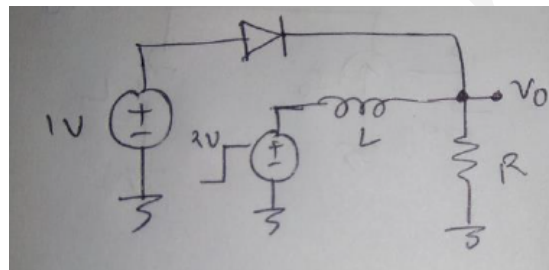
1. (a) Find the order of the circuit with and without capacitor C .
- (b) Draw V_{out} and find the steady-state current through R , with and without capacitor C .



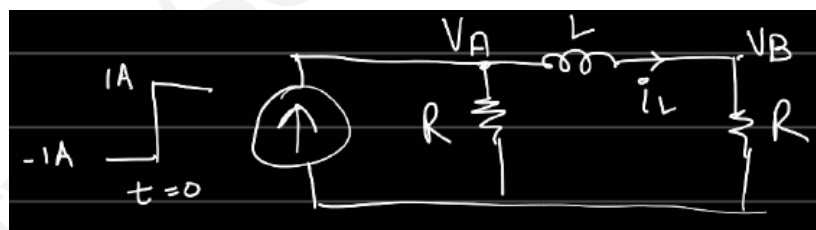
2. Draw V_o



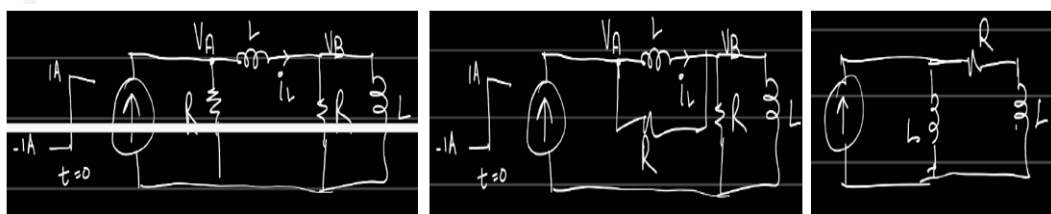
3. Draw the output waveform intuitively.



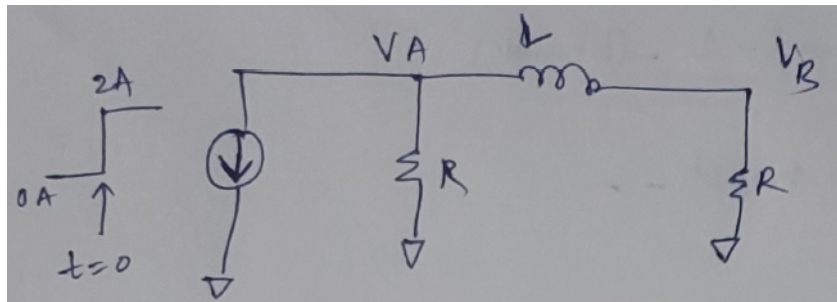
4. Find V_o at steady state. Plot V_A , V_B , and i_L .



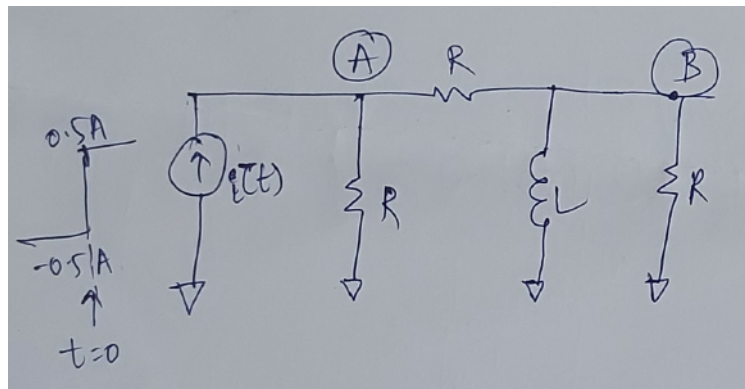
5. Plot V_A , V_B , and i_L .



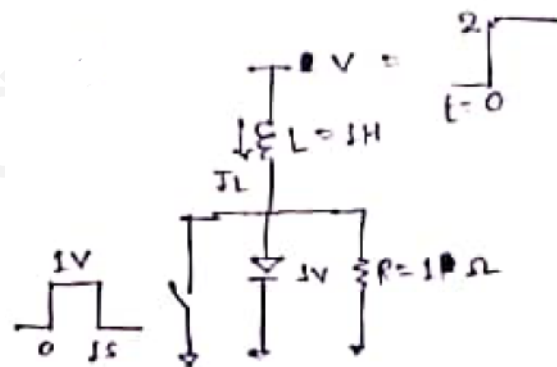
6. Plot V_A , V_B , and i_L . Find the time constant. (Observe the direction of the current source in the circuit.)



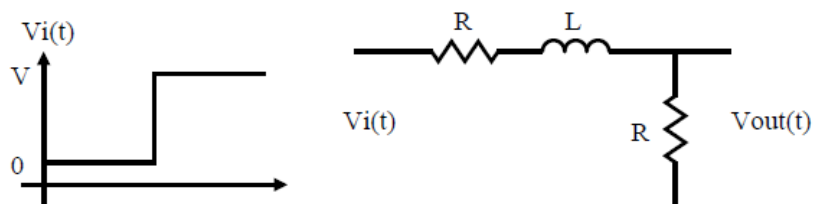
7. Plot V_A , V_B , and i_L .



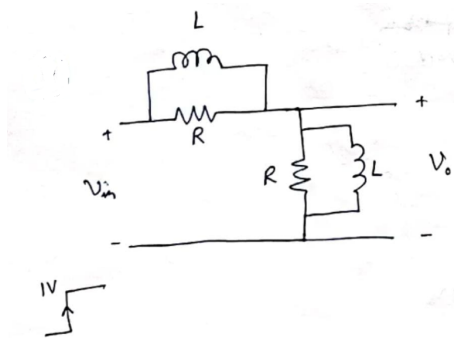
8. Given: $L = 1 \text{ H}$, $R = 1 \Omega$, diode on-voltage = 1 V . A 1 V pulse is applied to the switch from $t = 0$ to $t = 1 \text{ s}$. A 2 V step is applied at $t = 0 \text{ s}$ to V (or V_{DD}).
- $I_L(t = 2 \text{ s}) = ?$
 - Plot $I_L(t)$.
 - Find the slope of I_L between $t = 1 \text{ s}$ and $t = 2 \text{ s}$.



9. For the given circuit, plot the inductor current $i_L(t)$ and the inductor voltage $V_L(t)$.



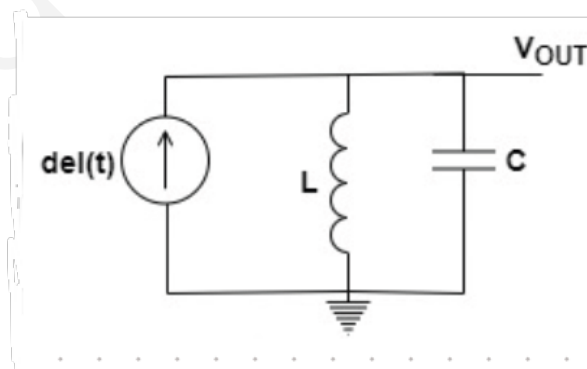
10. (a) Plot the output voltage V_o .



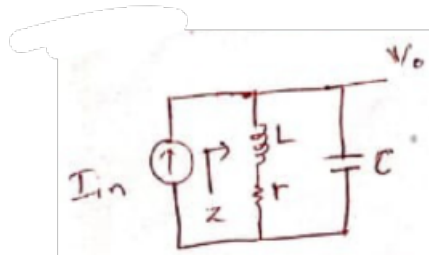
- (b) Determine the time constant of the circuit.
 (c) If the circuit has a finite time constant, explain why the output V_o resembles a step voltage.
 (d) Alternatively, an interviewer may ask:
 Using the calculated time constant, draw the Bode plot of the circuit.
 (e) Follow-up question:
 (Assume your answer indicates a low-pass filter characteristic.) If the circuit exhibits a low-pass filter response, why does the output contain all the frequency components of the input signal, despite the low-pass behavior?

1.4 RLC Circuits

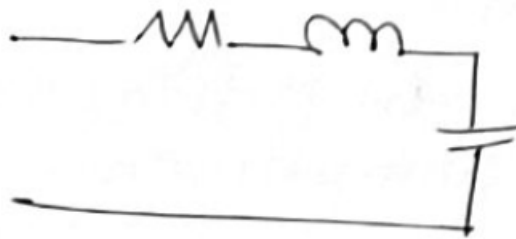
1. Why V_{out} is oscillating and at $t=0+$ what is the voltage across capacitor and without any mathematics justify how it will give sine waveform.



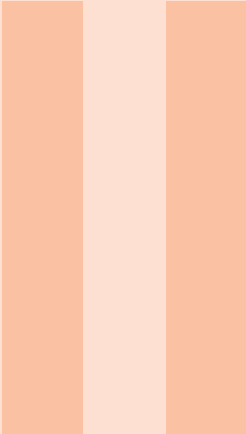
2. a. Draw the frequency response.
 b. Indicate the slopes in the response.
 c. Determine the impedance Z at resonance.
 d. Calculate the quality factor (Q).
 e. Identify the peak of the frequency response plot.



3. Plot the frequency response.



4. Draw the Bode plot for the complex pole $s = -1 + 10j$.



Active Circuits

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8.1	Prerequisites	
8.2	Questions	

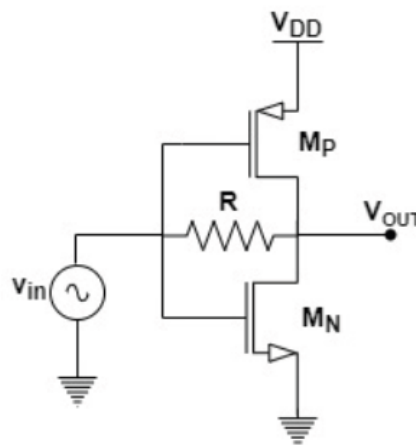
2. Single Stage Amplifiers

2.1 Prerequisites

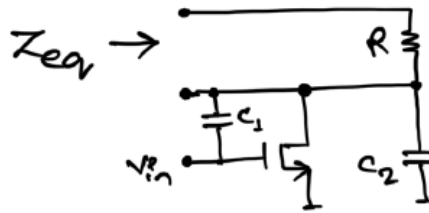
1. Razavi Electronics 1 by Prof. Behzad Razavi
2. Razavi Electronics 2 by Prof. Behzad Razavi
3. Electronics – Analog IC Design by Prof. Nagendra Krishnapura
4. Chapters 1–5 from the textbook *Design of Analog CMOS Integrated Circuits* (2nd Edition) by Behzad Razavi
5. MOS Structure and MOSCAP — Das Sir (Initial lectures – deep explanation at design level)

2.2 CS,CD,CG amplifiers

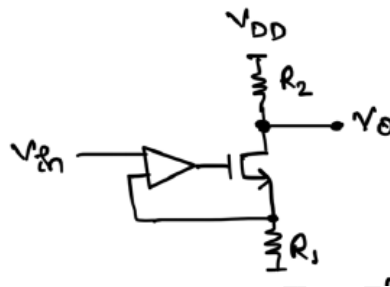
1. Find overall gain?



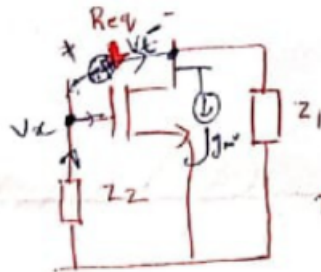
2. Find out the equivalent impedance.



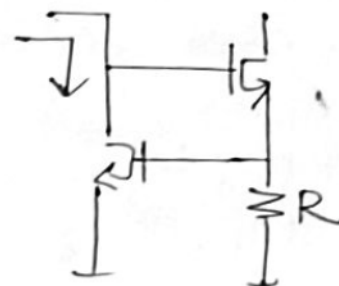
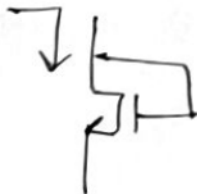
3. Find the opamp terminals for negative feedback. then find V_o .



4. Find the equivalent resistance R_{eq} . Replace Z_1 and Z_2 with capacitors C_1 and C_2 , respectively, and determine the new equivalent resistance R_{eq} .

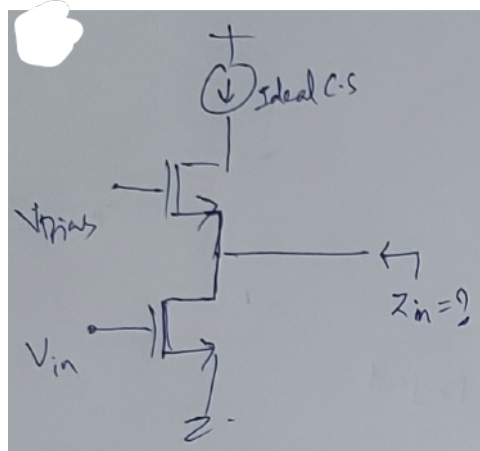


5. Find Z_{in} in all three cases (let $\lambda = 0$).

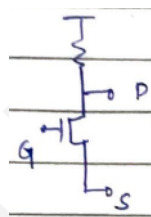


6. Find the gain and plot the frequency response of common-source (CS), common-drain (CD), and common-gate (CG) amplifiers.
7. Explain channel length modulation from a device-level point of view.

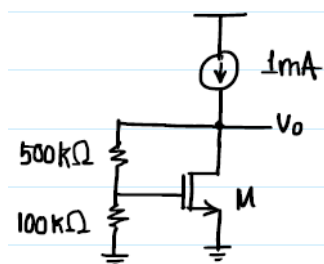
8. Find Z_{in} ? (You are not allowed to use the small-signal circuit. You should answer without lengthy math.)



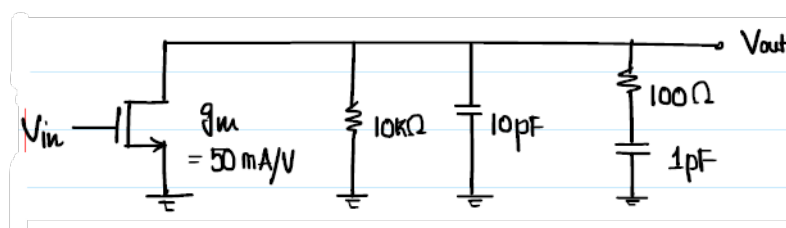
9. Draw the common-source (CS) amplifiers you know. After drawing them, explain the differences between the circuits and the reasons for moving from one circuit to another.
10. Voltage drop across drain to source for large values of V_{GS} .



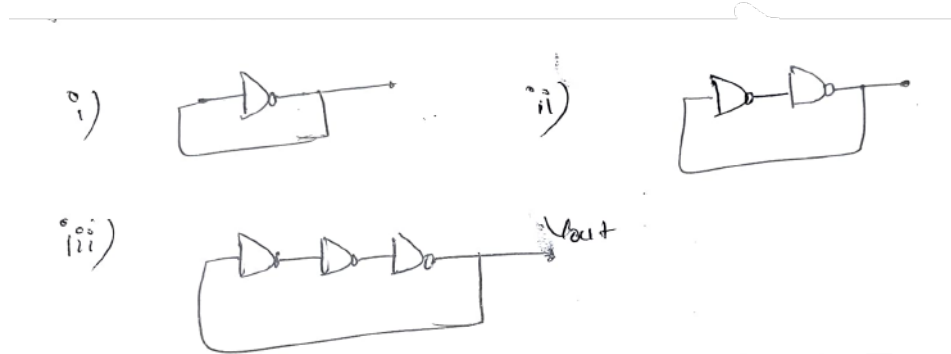
11. When the overdrive voltage $V_{OV} = 100 \text{ mV}$, $I_D = 100 \mu\text{A}$, and $V_{th} = 0.1 \text{ V}$, determine V_o . (Do not solve it with unnecessary lengthy calculations.)



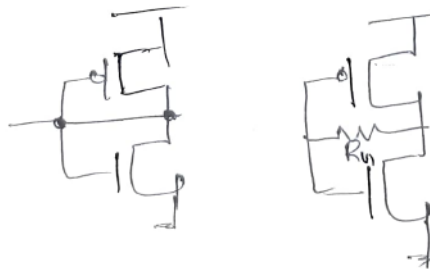
12. (a) Draw the frequency response.
(b) Find the locations of the poles and zeros.



13. (a) Draw the inverter characteristics.
 (b) Design an inverter such that the output will be high for an input voltage of 1V. $V_{DD} = 3V$.
 (c) Draw the output of the three circuits shown below.



- (d) Can we use an inverter as an amplifier? If yes, how?
 (e) Where should it be biased, and how should it be biased? (Answer: Place a resistor between input and output.)
 (f) What is the difference between the circuits shown below?

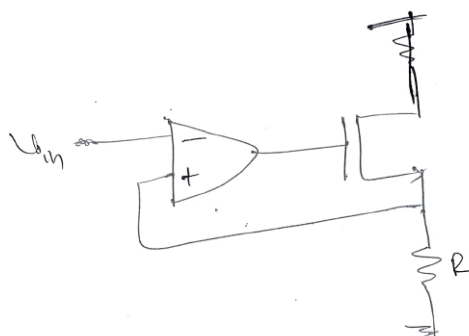


14. Do you recognize this circuit? What is the name of the circuit? Explain its working principle.

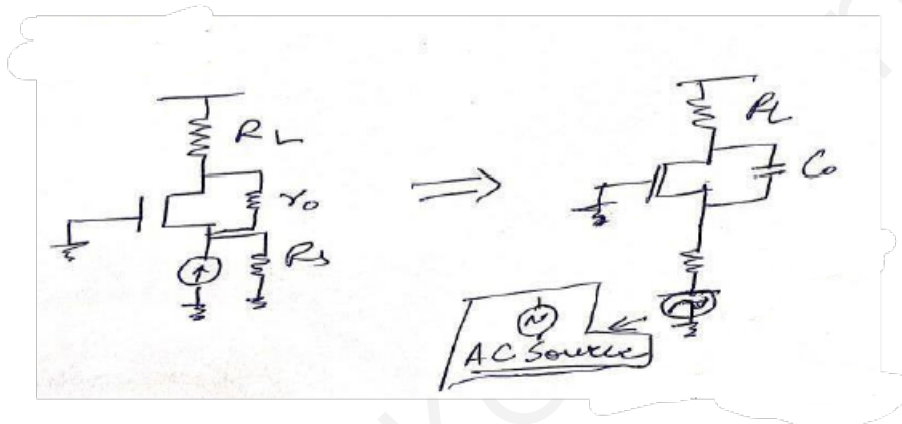
Note: The figure provided may contain an error. Either the op-amp terminals need to be reversed, or the transistor should be a PMOS instead of an NMOS for the circuit to function correctly.

Analyze the operation of the circuit under the following two scenarios:

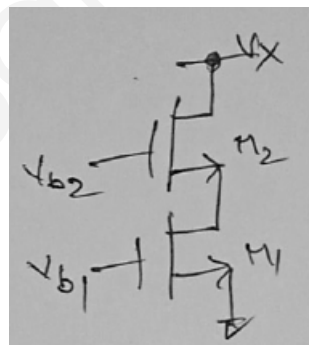
- (a) When the op-amp terminals are reversed.
 (b) When a PMOS transistor is used in place of the NMOS transistor.



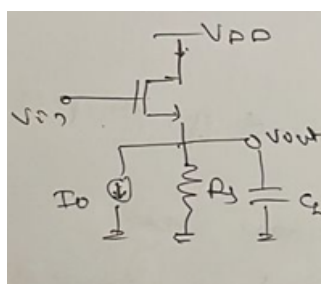
15. (a) Draw a simple amplifier.
 (b) What is the gain?
 (c) How can the gain be increased? List different techniques and their limitations.
 (d) How can the bandwidth be increased?
16. What happens to V_{th} with an increase in temperature? Give an intuitive explanation.
17. Draw the cross-sectional view of a MOSFET and explain its structure. Why is specific doping used at particular regions for PMOS and NMOS devices? Explain the variation of capacitance under different operating conditions, and why these variations occur.
18. Draw a Common-Gate amplifier and explain its working and voltage gain. Convert the current source to a voltage source and set $R_s = 0$. Find the poles and zeros of this modified circuit.



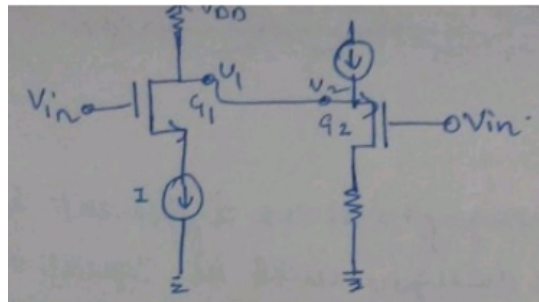
19. Which MOSFET will enter the triode region first if V_x decreases?



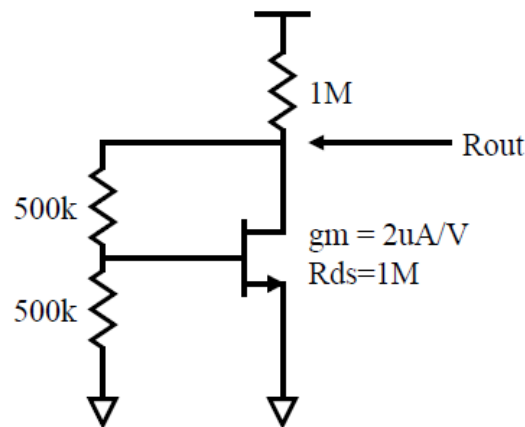
20. Draw the cascode amplifier and find its gain. List techniques to further increase the gain. Draw the gain-boosted circuit and find its gain.
21. a) Find the gain.



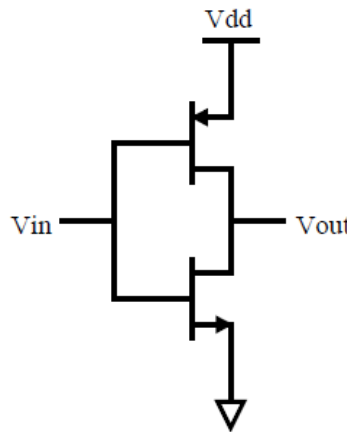
- b) Plot V_{out} for a pulse input.
 - c) Find the pole at the output.
 - d) Find the pole considering C_{gs} .
22. Write the current equation of a MOSFET in the triode region.
 23. How does the threshold voltage (V_{th}) change with an increase in temperature?
 24. How does the mobility (μ_n) change with an increase in temperature?
 25. What happens to the overall saturation current of a MOSFET if the temperature increases?
 26. Draw the cross-sectional view of an NMOS transistor. Show all the capacitances and determine their values.
 27. Without writing equations, explain how the body voltage affects the drain current (I_D) of a MOSFET.
 28. The gain of the NMOS transistor is G_1 , and the gain of the PMOS transistor is G_2 . If their outputs are shorted together, determine the resulting small-signal gain of the combined configuration.



29.
 - (a) Draw the cross-sectional view of an NMOS transistor structure, labeling all regions including the gate, source, drain, channel, oxide, and substrate.
 - (b) Explain the behavior of the NMOS transistor for the following gate-to-source voltage (V_{GS}) conditions:
 - $V_{GS} < 0$
 - $0 < V_{GS} < V_{th}$
 - $V_{GS} > V_{th}$
 - (c) Identify the key parameters that influence the threshold voltage V_{th} of an NMOS transistor.
 - (d) Discuss the impact on threshold voltage V_{th} when the body voltage V_B is made positive as compared to when $V_B = 0$.
 - (e) Draw and label all the parasitic capacitances associated with the NMOS structure from part (a), including gate-to-source, gate-to-drain, and gate-to-body capacitances.
 - (f) Derive and present the expressions for the intrinsic capacitances in both the linear (triode) and saturation regions of operation.
 - (g) Define the pinch-off condition in an NMOS transistor. Explain how pinch-off affects the I_D vs. V_{DS} characteristics.
 - (h) Describe the relationship between channel length, output resistance r_o , and drain current I_D . Discuss how short-channel effects influence these parameters.
30. Calculate the output impedance of the given circuit.

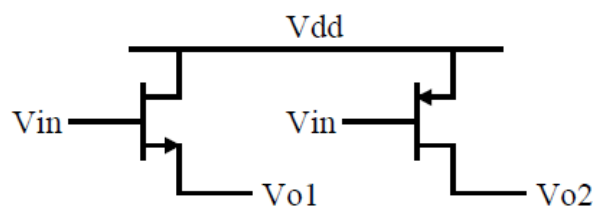


31. (a) If the inverter is biased at the midpoint of V_{DD} , what is its small-signal gain?

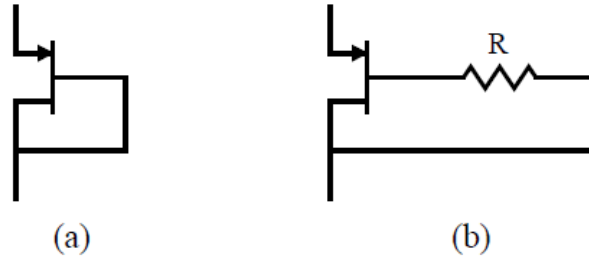


- (b) Draw the cross-sectional diagram of a CMOS inverter. Clearly indicate the contacts for power supply (V_{DD}) and ground (GND).
- (c) Using the cross-sectional diagram from part (b), illustrate how parasitic BJTs can form within the structure, potentially leading to latch-up.
- (d) Describe the methods used to prevent latch-up in CMOS technology. Include techniques such as guard rings and clamping circuits.
- (e) Draw the layout of a CMOS inverter or a standard logic gate such as NOR or NAND. Clearly label the PMOS and NMOS regions, polysilicon gates, diffusion areas, and metal interconnects.
32. For the given circuits with $V_{DD} = 5\text{ V}$, determine the output voltages V_{o1} and V_{o2} for the following input voltages:

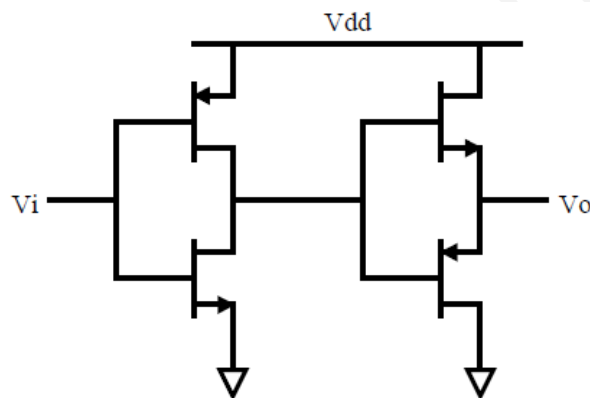
$$V_{in} = 5\text{ V}, \quad 3\text{ V}, \quad 2.5\text{ V}, \quad 0\text{ V}.$$



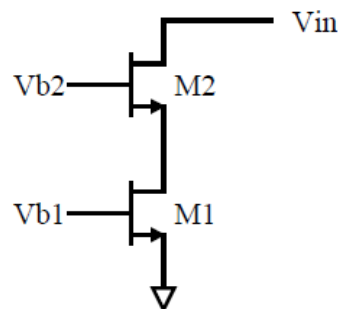
33. What is the effective resistance from source to drain for each of the following two transistors? (Assume the given resistance value is R .)



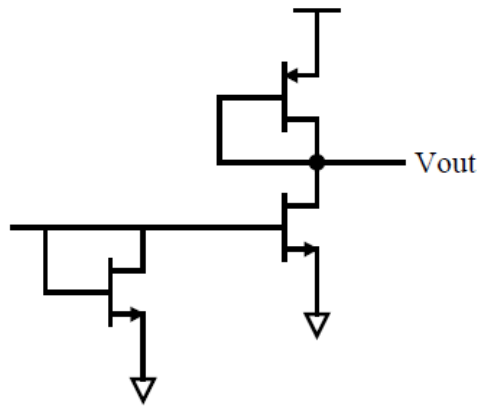
34. For the given circuit, if the input V_i is a rail-to-rail square wave, sketch the waveform after the inverter and the output V_o . Assume V_{DD} is the supply voltage.



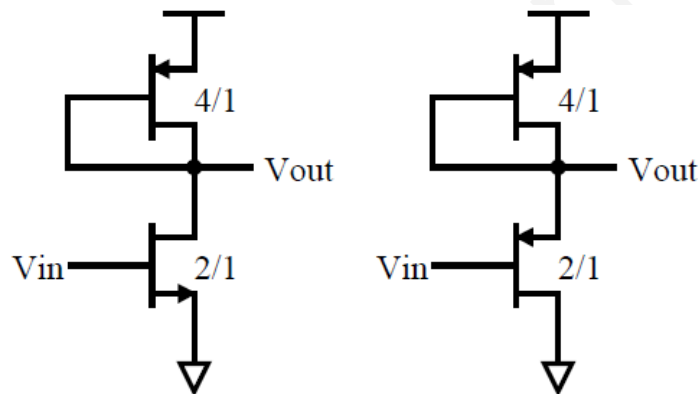
35. For the following circuit, the threshold voltage of the transistor is 0.7 V. Given $V_{B1} = 1$ V and $V_{B2} = 2$ V, plot the current flow through the transistors as a function of the input voltage V_{in} , as V_{in} varies from 5 V to 0 V. (This question was provided by Wang Ge.)



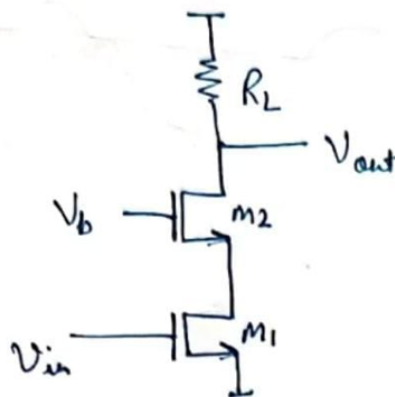
36. For the following circuit, the small-signal input is I_{in} and the small-signal output is v_{out} . Determine the small-signal output expression and calculate the corresponding gain.



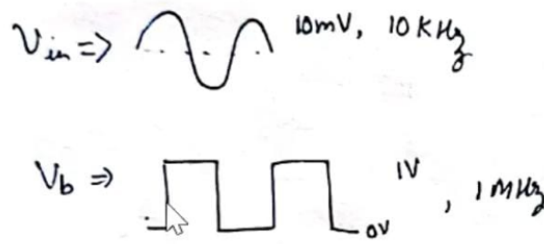
37. Determine the gain of the following circuit. Assume the electron mobility $\mu_n = 2\mu_p$, where μ_p is the hole mobility.



38. (a) Determine the gain of the circuit.



- (b) What is the output voltage (V_{out}) for the given input signals V_{in} and V_b ?

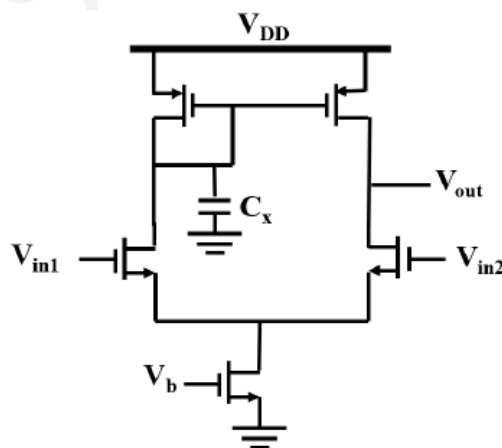


- (c) Draw the output frequency spectrum, clearly marking the exact magnitudes of each component.

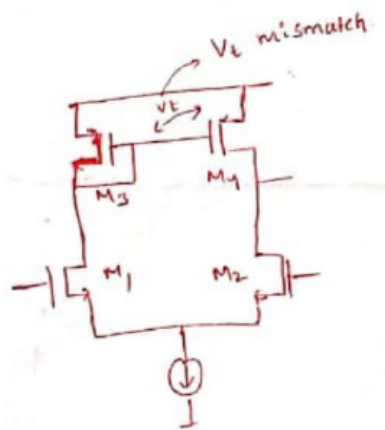
Hint: Use the Fourier transforms of sine and square waves.

2.3 5T-OTA Analysis

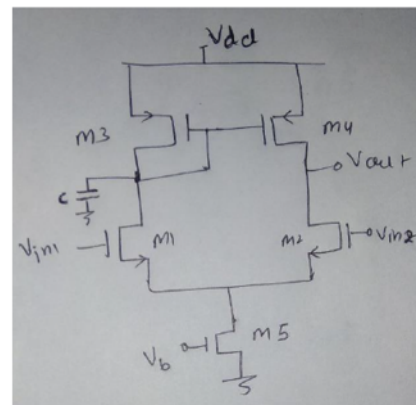
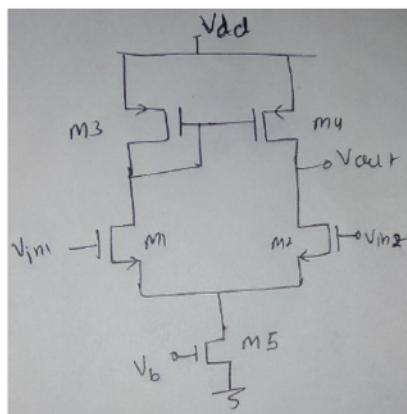
1. If load and parasitic capacitance are not present at V_{out} in the 5T-OTA shown below:
 - (a) What happens to the pole at V_{out} ?
 - (b) Now, what is the dominant pole?
 - (c) Draw the frequency response without using any mathematical calculations. Explain qualitatively.
 - (d) Find the Norton's equivalent current.



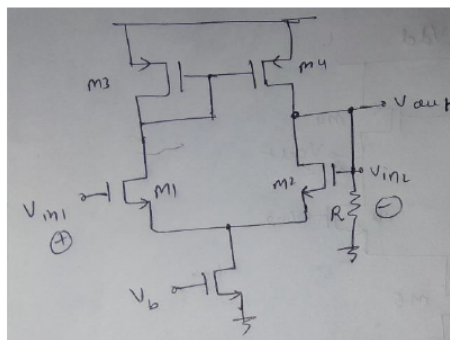
2. Draw a 5T-OTA and a folded cascode op-amp. What happens if there is a mismatch in the threshold voltage (V_{th}) of the NMOS and PMOS transistors in both circuits?
3. For the output offset to be zero, what is the required input offset when there is a threshold voltage (V_{th}) mismatch between transistors M_3 and M_4 ?



4. (a) Find the gain of the circuit.
- (b) Determine the input common-mode range (ICMR) and output swing of the circuit.
- (c) How do you connect the circuit so that it becomes a unity follower? Find its step response.
- (d) Find the transfer function in the mid-frequency range after adding the capacitor C .



5. Draw the step response of the circuit.

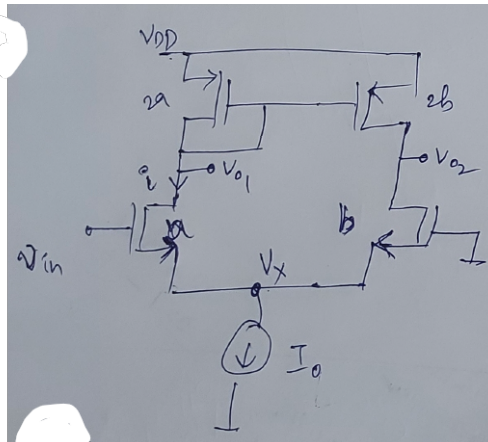


6. Let a , b , $2a$, and $2b$ be transistor names. The r_{ds} of all transistors is neglected.

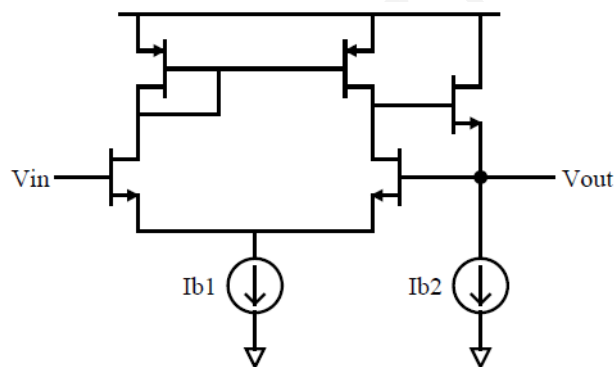
Hint: You may assume i is the signal current through transistor a .

- (a) Find the signal current through all transistors. With r_{ds} , what is the signal current through r_{ds2b} ?

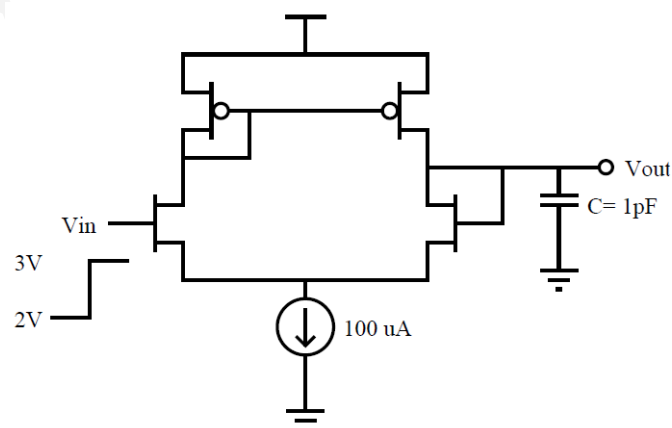
- (b) Find V_x , V_{o1} , and V_{o2} when V_{in} is a small signal.
 (c) What happens if the signal is applied at the V_{DD} node? Find V_x , V_{o1} , and V_{o2} .



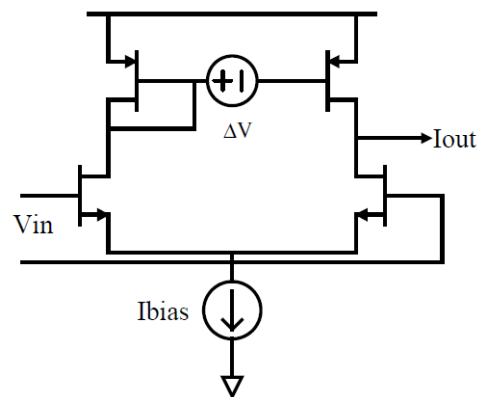
7. For the following circuit, determine the voltage gain $\frac{V_{out}}{V_{in}}$. Identify the location of the feedback and explain its function within the circuit.



8. Determine the slew rate of the output voltage for the given circuit or system.

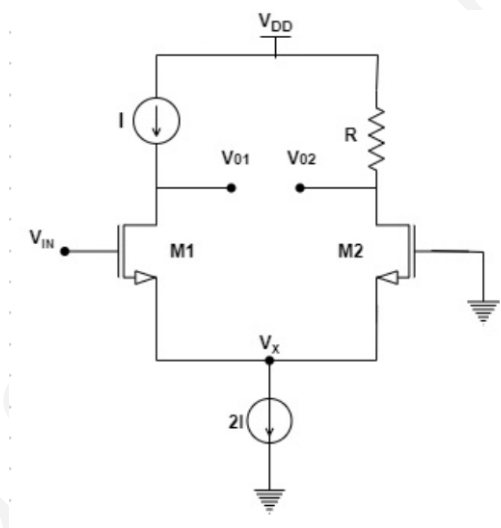


9. Calculate I_{out} as a function of V_{in} , g_{mn} , g_{mp} , and ΔV .

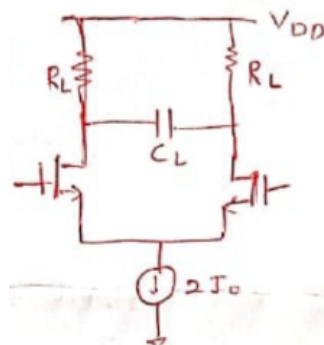


2.4 Differential Amplifiers

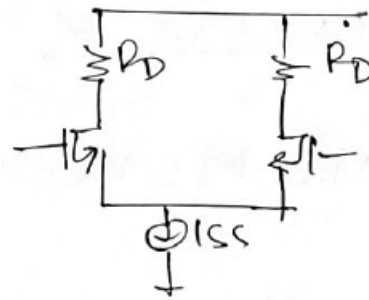
1. Draw V_{O1} , V_{O2} , and V_x versus time (t) for a large V_{IN} signal. Assume all current sources are ideal.



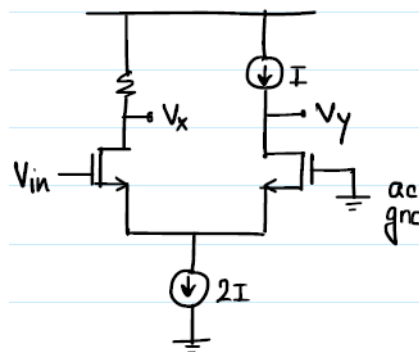
2. Find the DC gain and the unity-gain bandwidth (UGB).



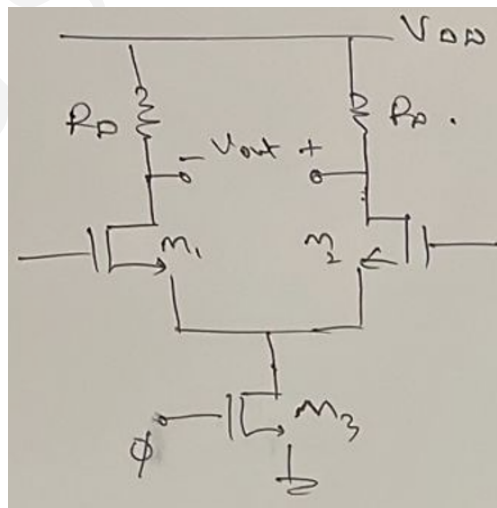
3. If $g_{m1} \neq g_{m2}$, what will be the value of $\frac{A_{o,dm}}{A_{i,cm}}$ for the circuit?



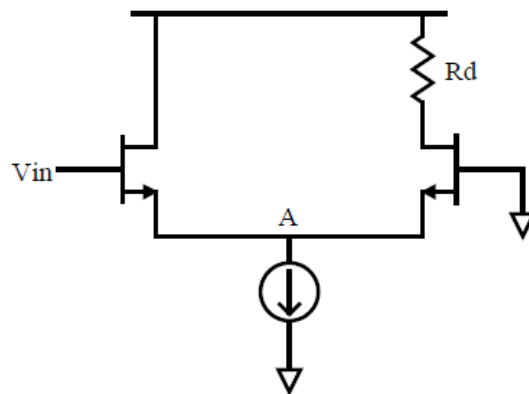
4. Determine $\frac{V_x}{V_{in}}$ and $\frac{V_y}{V_{in}}$. Assume channel length modulation.



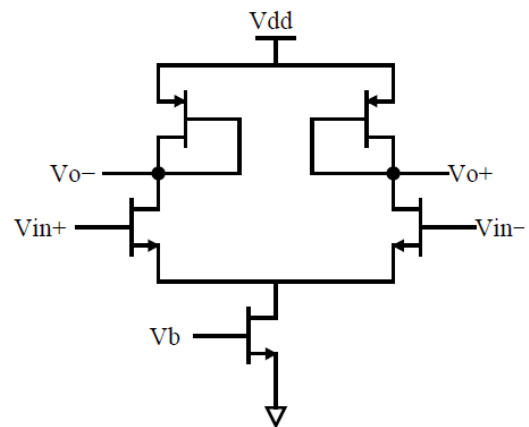
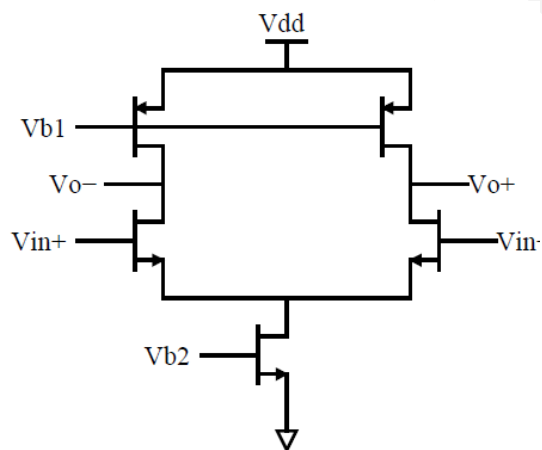
5. (a) Draw an op-amp circuit using MOSFETs.
 (b) In a differential amplifier with a tail current source and resistive load R_L , how can we replace the current source and R_L with other circuitry? Can R_L be replaced by a BJT?
 6. a) Find $ICMR_+$ and $ICMR_-$.



- b) What happens if M_3 is a practical current source?
 c) Analyze the circuit with R_D mismatch.
 7. Both transistors are biased in the saturation region. Calculate the ratio $\frac{V_A}{V_{in}}$, neglecting the body effect.



8. (a) What is the voltage gain of each circuit?
 (b) What technology or layout technique can be used to improve the matching of the input transistors?
 (c) If the bias current is increased, what effect does it have on the gain? (*Hint: Gain decreases!*)
 (d) What happens to the bandwidth when the bias current is increased?
 (e) List the advantages and disadvantages of the two amplifier configurations shown.
 (f) Now replace the NMOS transistors with NPN BJTs, and the PMOS transistors with PNP BJTs. Answer the above questions again for this bipolar implementation.
Note: In this case, the gain remains approximately constant with increasing bias current.





3. Two Stage OP-amp

3.1 Prerequisites

1. Feedback and Stability by Analog Snippets
2. Analog IC Design by Prof. Nagendra Krishnapura

3.2 Questions

1. Explain the design procedure of a two-stage operational amplifier.
2. Explain the working of the circuit.
3. What is compensation?
4. Why is Miller compensation used?
5. What do you mean by unity gain bandwidth?
6. Does the unity-gain frequency change after a Miller capacitor is added?
7. Write the expression for the Unity-Gain Bandwidth (UGB).
8. What are the locations of the poles and zeros?
9. How are mirror poles and zeros formed?
10. Where is the second pole located? Explain how its value is derived.
11. Explain pole splitting and its issues.
12. What happens to the output impedance of the second stage after introducing the compensation capacitor (C_c)?
13. How can the CMRR be improved?
14. How can you improve the phase margin of the circuit?
15. How do you cancel the RHZ and derive the conditions?
16. How much is the effective capacitance at the mirror node?
17. What if there is a mismatch?
18. What do you mean by a common-mode signal?
19. Draw the unity-gain buffer configuration using an op-amp. If there is a mismatch in the

input transistors, what do you expect at the output?

20. How did you design the bias current values in the two stages? Should the overdrives of the bias current sources necessarily be equal?
21. How did you ensure that all MOSFETs are in saturation?
22. What are the critical noise sources?
23. Draw the internal structure of a two-stage op-amp. Identify the contributions of poles and zeros, and explain their effects. What parasitics contribute to the formation of mirror poles and zeros? Include the Bode plot of the same.
24. Explain the Miller Effect and the need for compensation in op-amps.
25. What is the slew rate?
26. What is the slew rate (SR) if the compensation capacitor (C_c) is not present?
27. Find the input voltage swing.
28. What is phase margin, and why is C_c used?

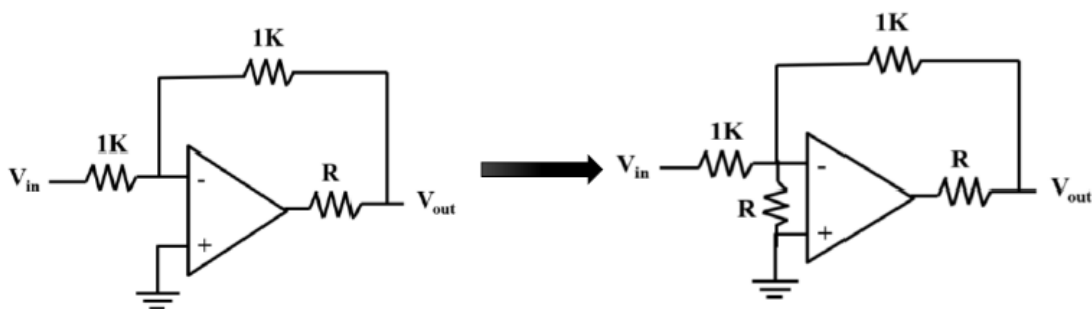
4. Op-amp Circuits

4.1 Prerequisites

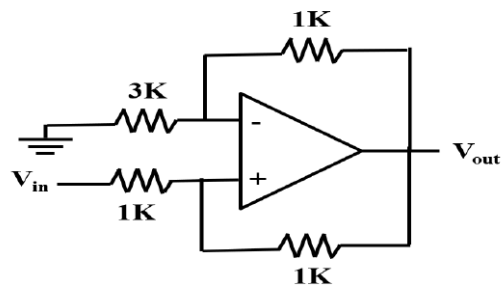
1. Analysis of Opamp Circuits by Chembiyan T
2. Prep for Interview by Himanshu Agarwal (Lectures 26 to 39)
3. Analog Electronics GATE Notes/Material

4.2 Questions

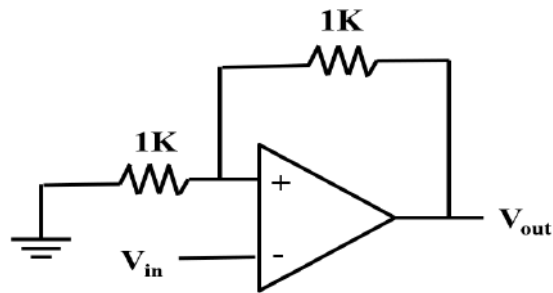
1. (a) Find the output resistance with and without R .
(b) Find the input resistance.
(c) Find the input and output resistance after R is added between the input terminals.



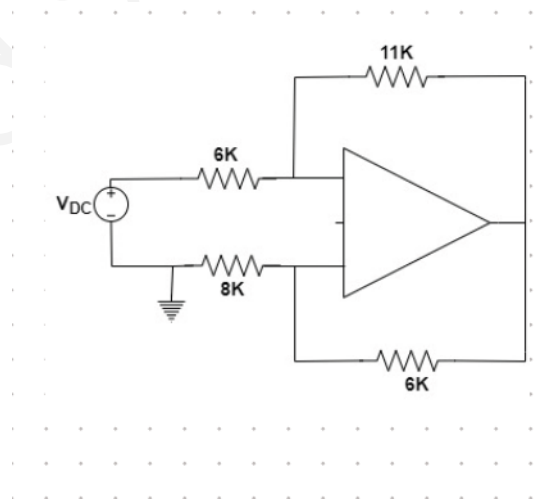
2. Find gain of the circuit?



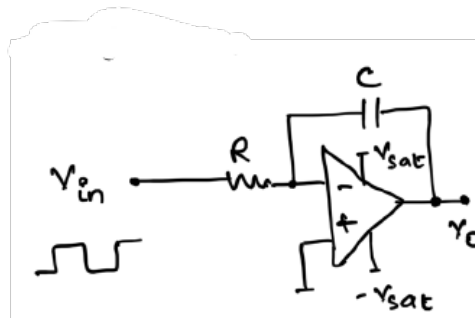
3. (a) Draw V_{out} vs V_{in} when V_{in} varies from -1 V to 1 V.
 (b) What is the value of V_{out} at $V_{in} = -\infty$?
 (c) Draw the hysteresis characteristics and find the trip points without using pen and paper.



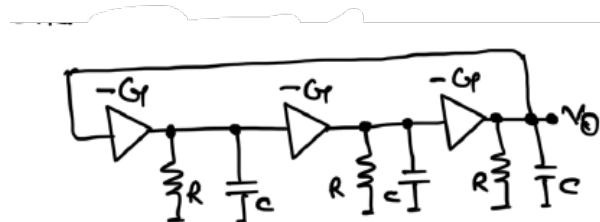
4. Mark the terminals of OP-amp for operating in negative feedback and find overall gain.



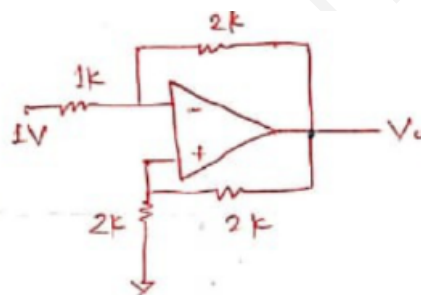
5. For the given circuit, plot the output response for the following cases: (i) $V_{sat} = \pm\infty$ (ii) $V_{sat} = \pm 15$ V.
 Moreover, if the duty cycle of the input is 60%, determine the rise time (t_{rise}) and fall time (t_{fall}) from the plot.



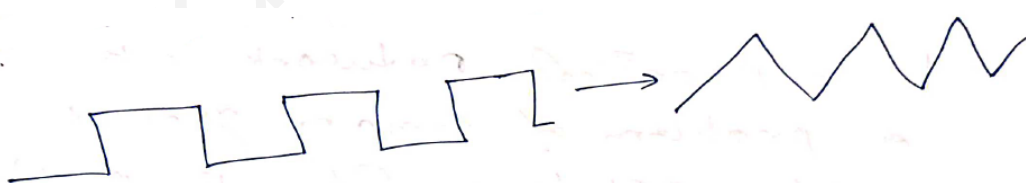
6. Find the condition for oscillation and the frequency of oscillation, where G is the gain of the circuit.



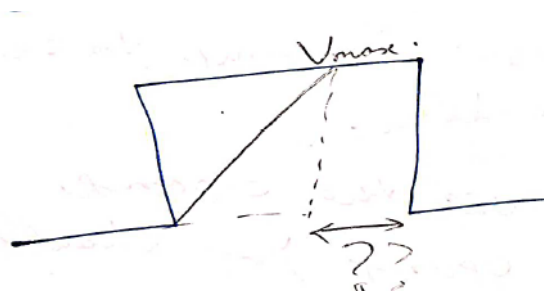
7. Find V_o .



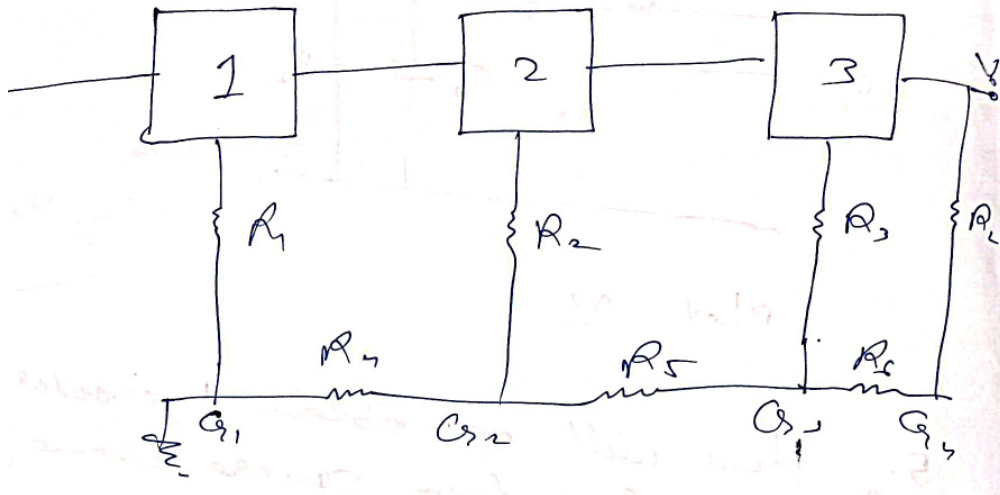
8. (a) How can you obtain a triangular wave from a square wave?



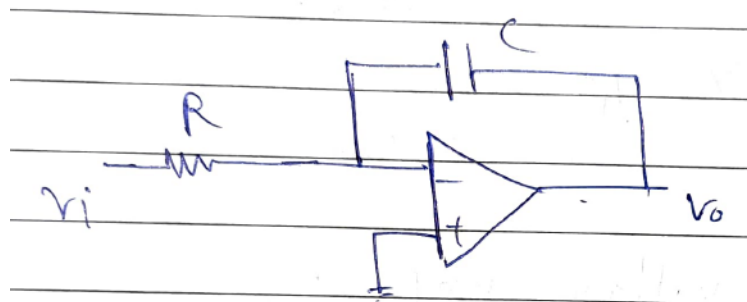
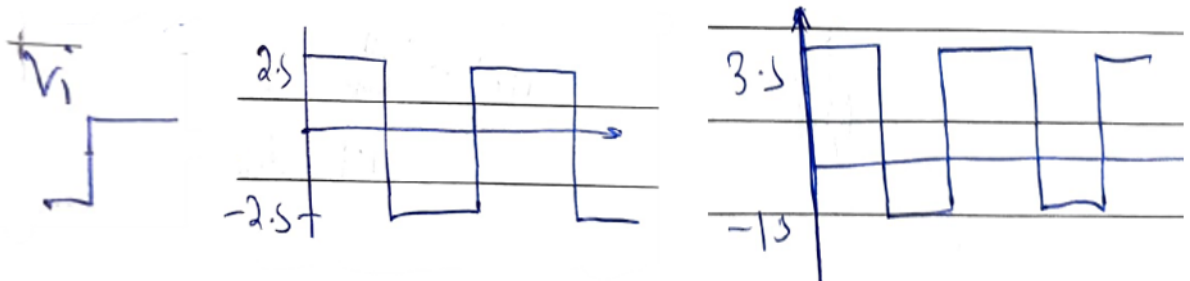
- (b) Consider that your answer is an op-amp integrator. What happens after V_o reaches V_{max} and the input still persists? Draw V_o for this situation.



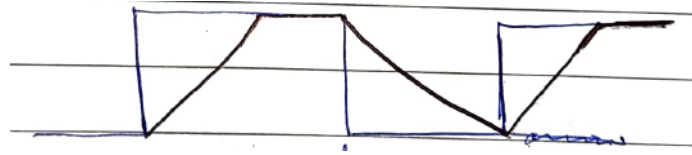
9. In a practical network, there is a problem with ground potential differences due to cable resistances (here, R_4 , R_5 , and R_6). All the ground nodes (G_1 , G_2 , G_3 , and G_4) have different potentials in practice. How can this problem be resolved? **Hint:** Use an op-amp to solve this problem. When using an op-amp, which feature of the op-amp should be considered most carefully?



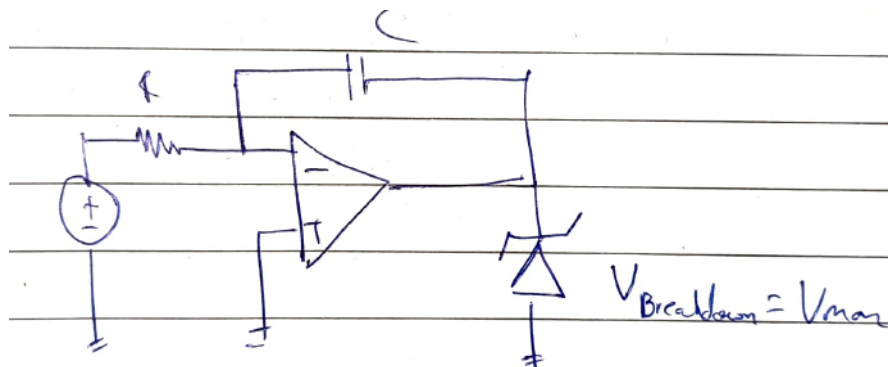
10. What will be the output voltage V_o for the given three input signals V_{i1} , V_{i2} , and V_{i3} ?



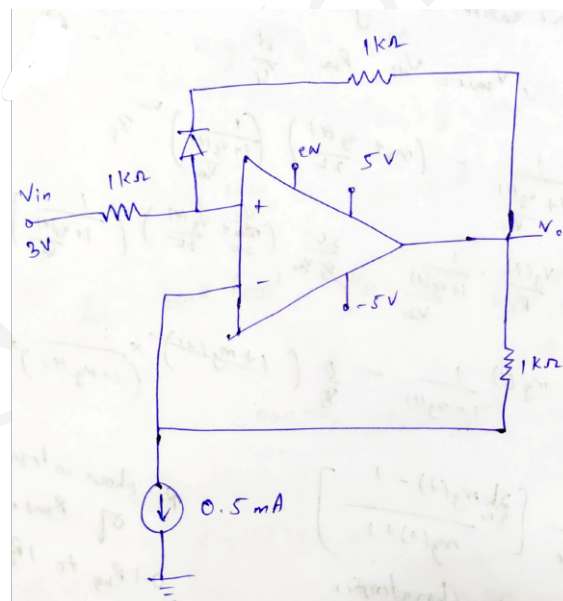
11. (a) Design a circuit to convert a given square wave to a trapezoidal waveform.
Hint: Use clipper circuits to clip the voltage at $V_{\max}$.



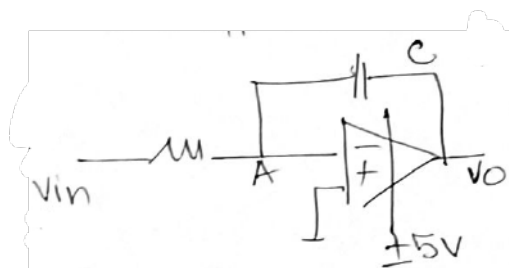
- (b) Determine whether the circuit shown below will function as intended to convert the square wave into a trapezoidal waveform.



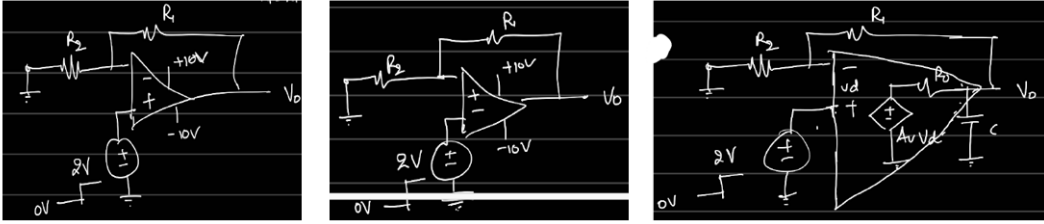
12. Assume an ideal diode with $n = 1$. What is the value of V_O ? Will the diode conduct at any point as the input voltage varies from 0 to V_{DD} ? Clearly explain the analysis.



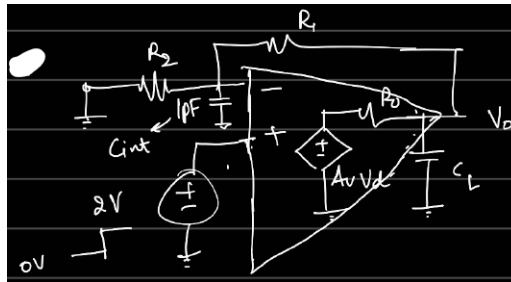
13. Plot V_O and V_A , and write the equation for $V_A(t)$.



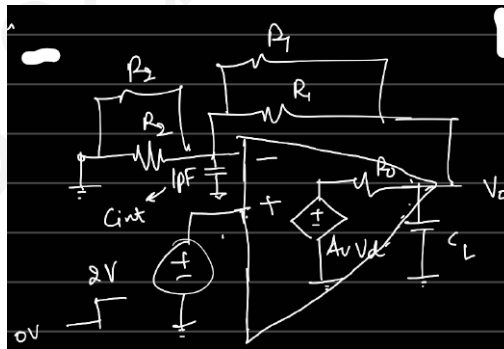
14. (a) Plot V_o and V^- .



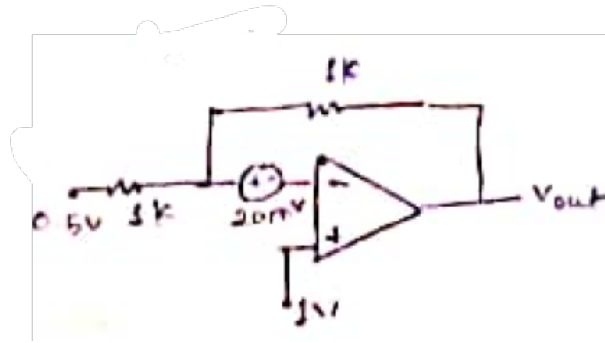
- (b) If τ_L (time constant due to C_L) $<$ τ_{int} (time constant due to C_{int}), then plot V_o and V^- .



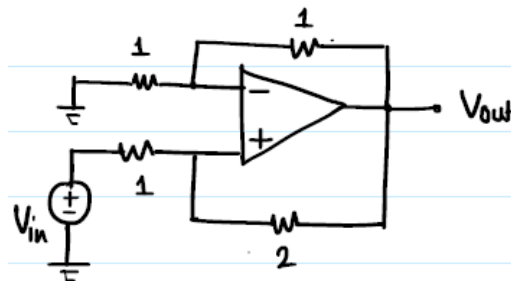
- (c) Plot the output of a second-order system (critically damped, over-damped, under-damped) in the time domain and relate to cases a and b.
- (d) Can you make the system critically damped? How? (**Hint:** Increase delay or decrease delay. We can decrease delay by decreasing R_1 , R_2 , but the feedback factor should not change, as shown in the figure below). Now plot V_o and V^- after R_{1eq} , R_{2eq} decrease. What are the issues in this approach?



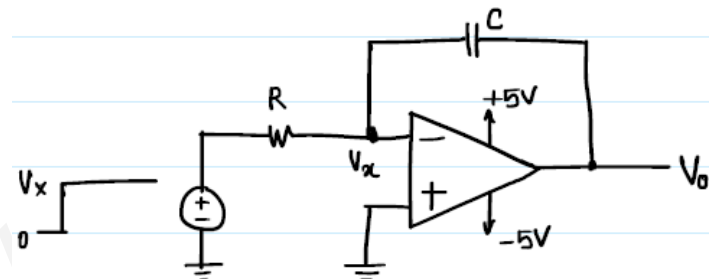
- (e) Let's say we have designed a mobile phone and it got rejected. Can you guess the reasons? (**Hint:** Battery lifetime / charging).
- (f) Now relate cases c–e to cases a and b. (Answer: more losses.) Cases c–e provide hints related to cases a and b.
15. A 20 mV offset is present at the inverting terminal. A 1 V is applied to the non-inverting terminal, and 0.5 V is applied to the inverting terminal side. All resistor values are $R = 1 \text{ k}\Omega$.
- Find V_{out} .
 - Find the output impedance.
 - Find the input impedance seen from the 0.5 V source.



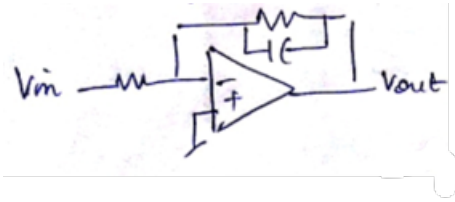
16. (a) Determine the gain.
 (b) Find the input impedance.
 (c) What if the input were a current source?



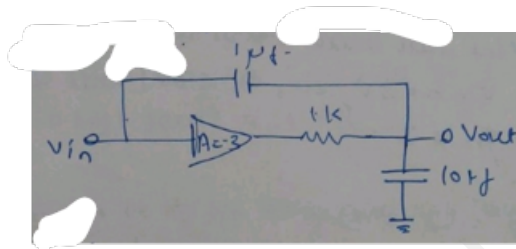
17. Assume finite loop gain. Plot V_x and V_o versus time.



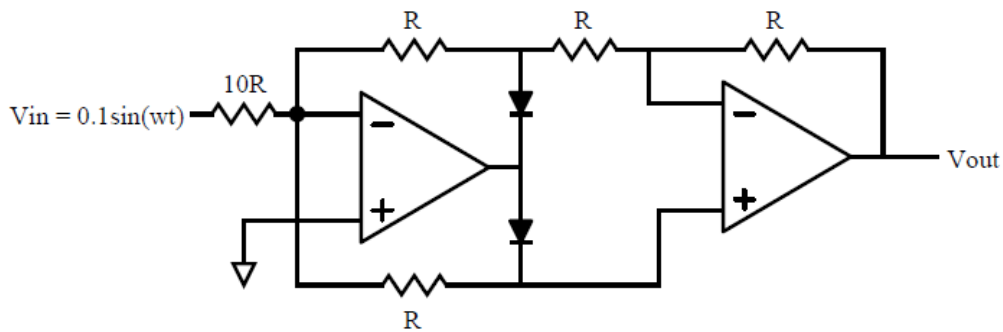
18. What is feedback? Explain.
 19. What are the conditions for oscillation? For a given loop, what happens to other frequencies? How is a particular frequency selected for oscillation?
 20. Why is a 60-degree phase margin typically chosen over other values?
 21. Explain the significance of Gain Margin and Phase Margin.
 22. What is loop gain, and how do we calculate or obtain the Bode plot during simulation?
 23. (a) Draw the latch circuit.
 (b) Draw the ring oscillator.
 (c) What is the Barkhausen criterion and what are its conditions?
 (d) Explain how oscillations are produced.
 (e) What is the loop gain at the start of oscillations and after the oscillations settle?
 (f) How does the loop gain decrease to 1?
 24. (a) What is the name of this circuit?



- (b) Plot V_{out} intuitively for step input.
 (c) Why do we prefer this over a conventional low-pass filter?
25. Determine the phase of the output waveform with respect to the input signal in the limit as the frequency approaches infinity.

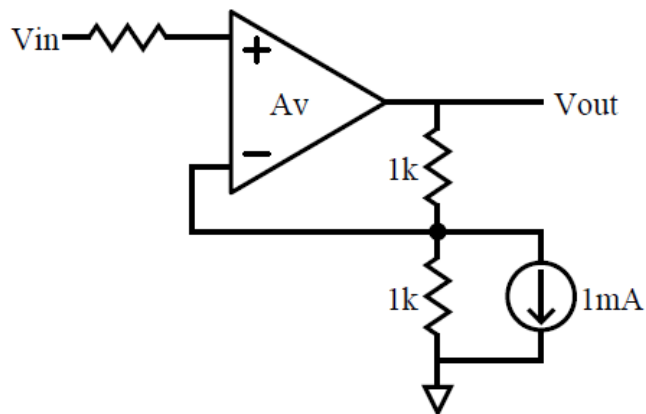


26. Plot the output voltage V_{out} .

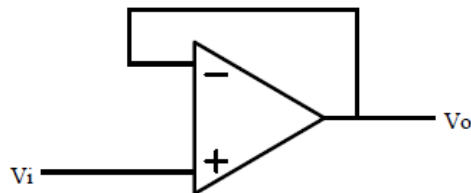


27. Calculate the output voltage under the following conditions:

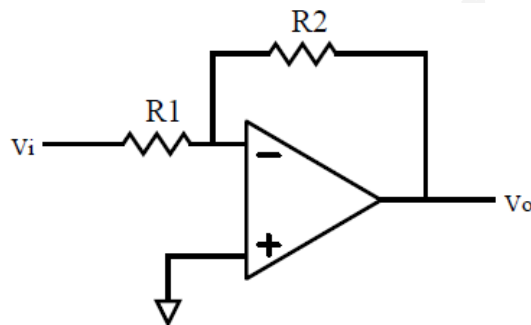
- (i) Voltage gain $A_v = \infty$
 (ii) Voltage gain $A_v = 10$



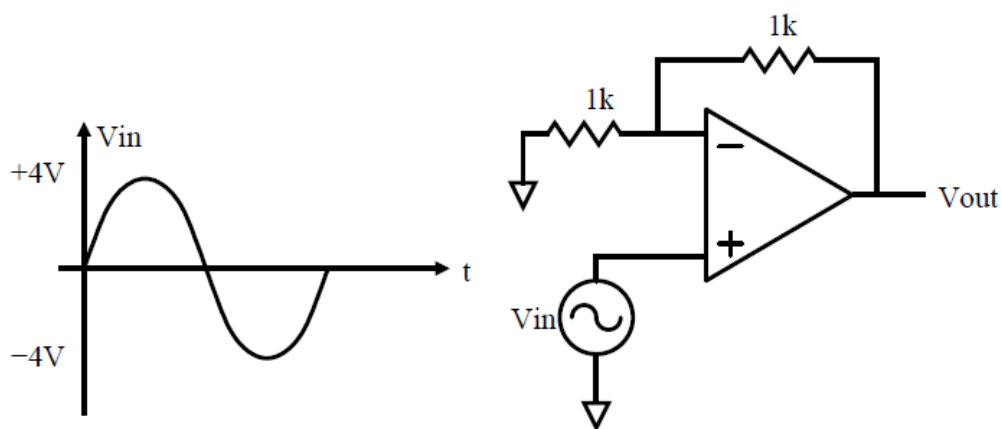
28. For the given source follower circuit:
- Determine its -3 dB bandwidth.
 - Analyze the stability of the circuit.



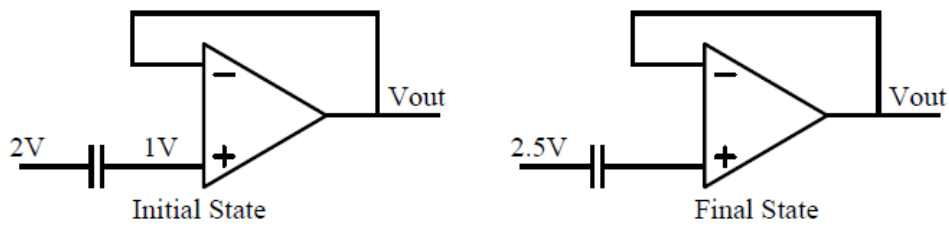
29. In the given circuit, if the two resistors are equal, determine the -3 dB bandwidth. Compare the stability of this configuration with that of a source follower.



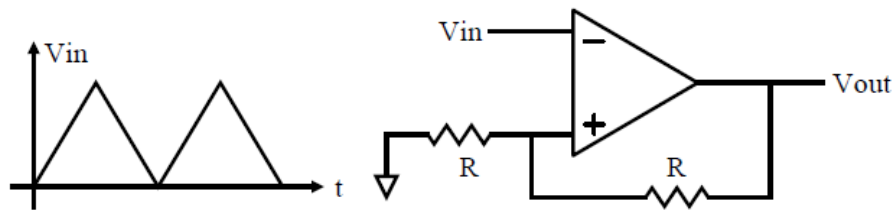
30. Sketch the output voltage V_o . Initially, $V_o = +5$ V. Assume the saturation voltage $V_{OSAT} = 5$ V.



31. Determine the final steady-state value of the output voltage V_{out} .

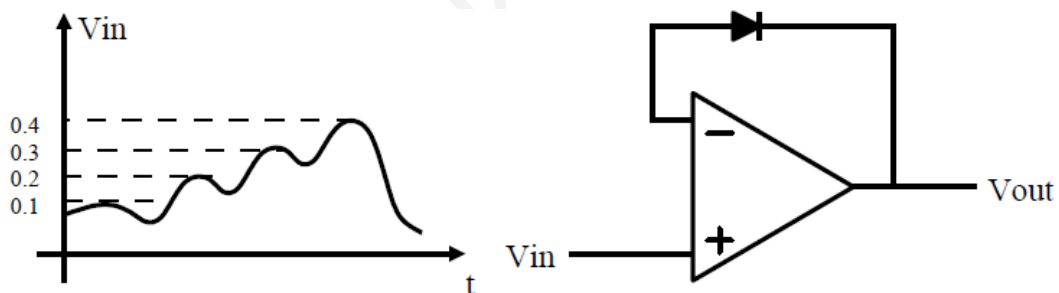


32. Plot the output voltage.

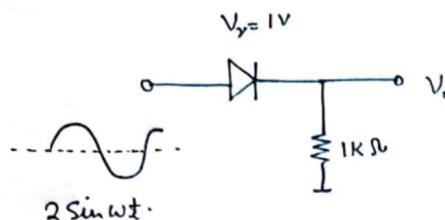


33. The frequency response of an open-loop operational amplifier is provided. The op-amp is configured as an inverting amplifier with a gain of -2 . Plot the corresponding closed-loop frequency response.

34. Plot V_{out} .



35. (a) Sketch the output voltage waveform V_o .



(b) Design a circuit that produces an ideal half-wave rectified output using a practical diode. Replace the practical diode with an appropriate configuration to achieve ideal half-wave rectification.

Hint: Use an op-amp in combination with a practical diode to implement an ideal rectifier.

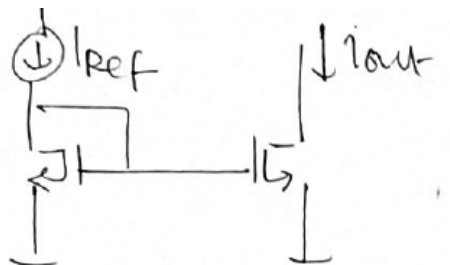
5. Current Mirrors

5.1 Prerequisites

1. Razavi Electronics II by Prof. Behzad Razavi (Lectures 1 to 6)
2. Mismatch in current mirrors:
 - Analog Snippets – Mismatch in Current Mirrors
 - SSCD – IIT Kanpur: Mismatch and Noise Concepts
3. Chapter 5 from the textbook *Design of Analog CMOS Integrated Circuits*, 2nd Edition by Behzad Razavi

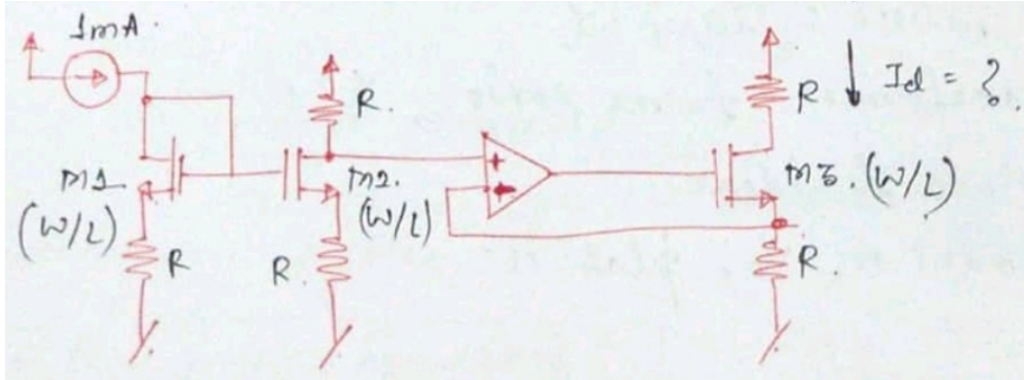
5.2 Questions

1. (a) Will $I_{\text{out}} = I_{\text{ref}}$? If not, why? What can be done to make $I_{\text{out}} = I_{\text{ref}}$? Plot voltage (V_{DS}) vs. current (I_{out}).

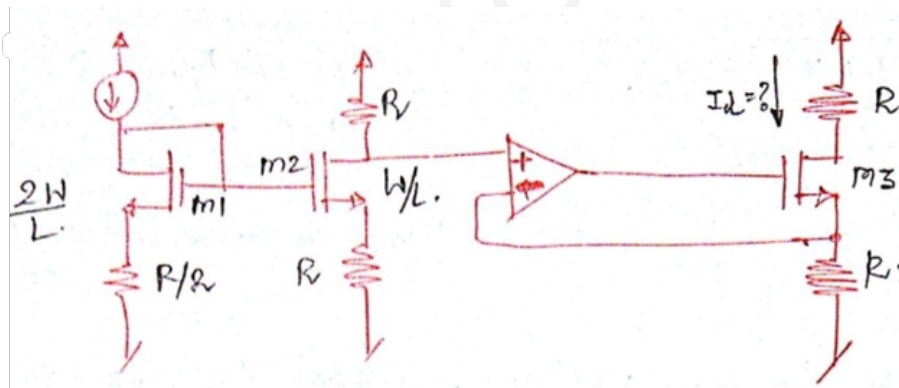


- (b) How are MOS devices sized for a high-swing cascode current mirror?
 - (c) Suppose I want $I_{\text{out}} = x \cdot I_{\text{ref}}$. What changes need to be made? Will it affect anything if the $\frac{W}{L}$ ratio is adjusted accordingly?
 - (d) What is the mismatch due to threshold voltage (V_t) in a current mirror?
2. (a) What is the effect of r_o in a current mirror?

- (b) How can mismatch in currents be reduced?
3. Draw the current mirror, explain it, and provide remedies for β mismatch, V_{th} mismatch, and V_{DS} mismatch considering channel length modulation.
 4. Draw the system-level diagram. If we want to obtain a current mirror with a 1:10,000 ratio, how will it be implemented?
 5. (a) What is I_D if the current source provides a constant current of 1 mA?

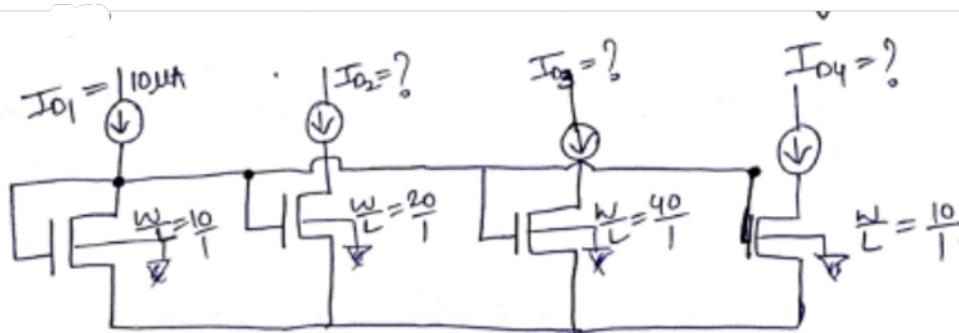


- (b) The MOSFET M1 now has a new aspect ratio of $2W/L$, and the resistor connected to the source is changed to $R/2$. Comment on I_D .

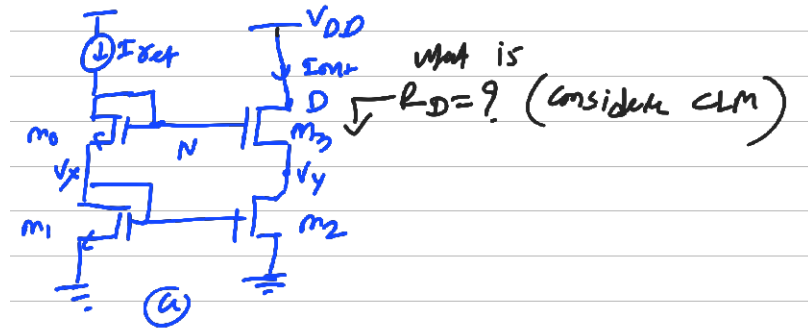


The interviewer continued this question with more focus on the new current mirror functions, and how this change is going to affect the current.

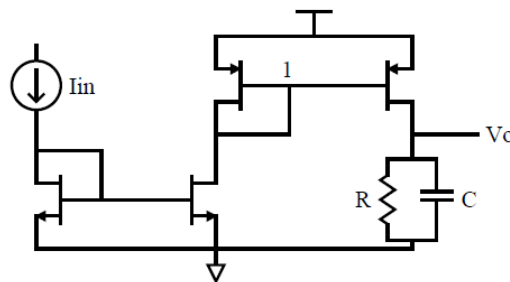
6. Find I_{D2} , I_{D3} , and I_{D4} .



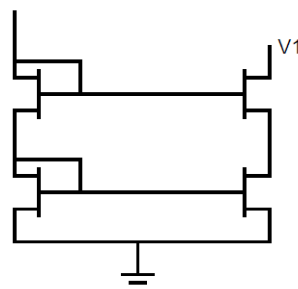
7. (a) Do you know the current mirror circuit? Draw it.
 (b) What conditions must be satisfied for proper current mirroring?
 (c) Why is a diode-connected MOS transistor used in the current mirror?
 (d) Considering channel length modulation (CLM), what problem arises, and how can it be mitigated?
 (e) How do you ensure that $V_x = V_y$? Prove your method.



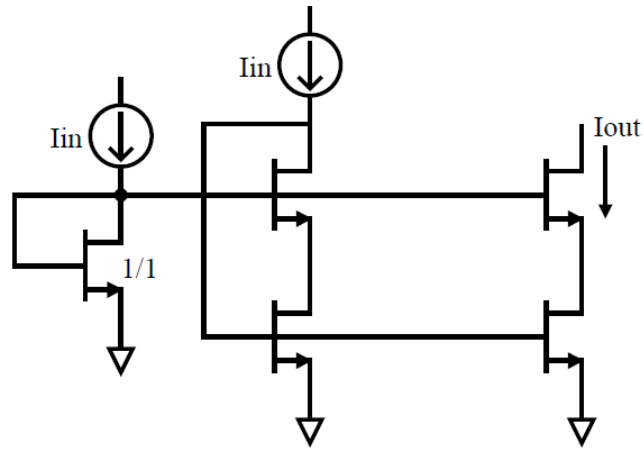
- (f) How can the gain of an operational amplifier be increased without increasing the output resistance R_{out} ? Provide a method independent of temperature and process variations. (Hint: Gain boosting)
 (g) Draw the circuit and derive gain expressions with and without gain boosting.
 (h) Explain how the method in part (g) can be applied to ensure $V_x = V_y$ in the circuit from part (e).
 8. Determine the low-frequency gain of the following circuits, where the input is the input current I_{in} . Identify the location of the dominant pole, and specify the position of the pole at node 1.



9. Determine the minimum value of V_1 required for the proper operation of the circuit.



10. Size the remaining four transistors in the circuit below such that $I_{\text{out}} = I_{\text{in}}$.



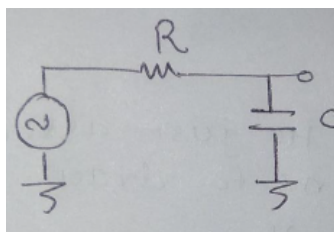
6. Noise Analysis

6.1 Prerequisites

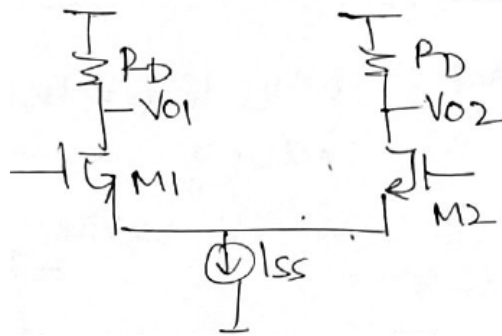
1. EE613A: High-Frequency Analog Circuit Design (2023) by SSCD IIT Kanpur (Lectures 29 to 33)
2. Noise in Electronic Circuits by Prof. Behzad Razavi
3. Chapter 7 (Noise) from the textbook *Design of Analog CMOS Integrated Circuits*, 2nd Edition by Behzad Razavi

6.2 Questions

1. Find the integrated noise spectral density onto the capacitor.



2. Only M_1 contributes noise to the circuit. What will be the value of V_{o1} and V_{o2} ?



3. (a) Draw a transimpedance amplifier.
- (b) Find the noise at V_o due to the resistor R . Assume the op-amp is ideal.



4. What are the different noise components associated with a MOSFET?
5. How can we obtain the noise voltage from the noise PSD?
6. Perform noise analysis of a 5T-OTA.
7. A system has an initial signal-to-noise ratio (SNR) of 60 dB. If an uncorrelated noise voltage of 1 mV is added to a signal of 1 V, what is the resulting SNR?

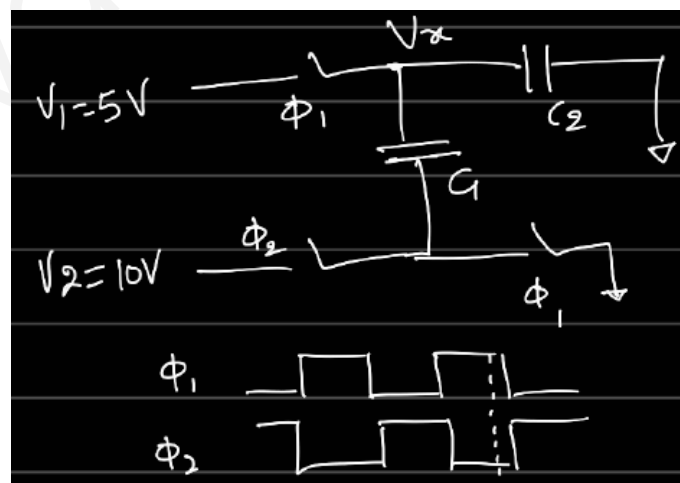
7. Switched Capacitor Circuits

7.1 Prerequisites

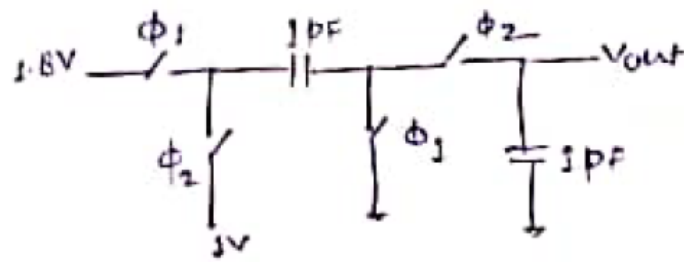
1. A Very Basic Introduction to Switched Capacitor Circuits by Chembiyan T
2. EE698I: Mixed-Signal IC Design (2024) by SSCD IIT Kanpur (Lectures 4(3) to 9)

7.2 Questions

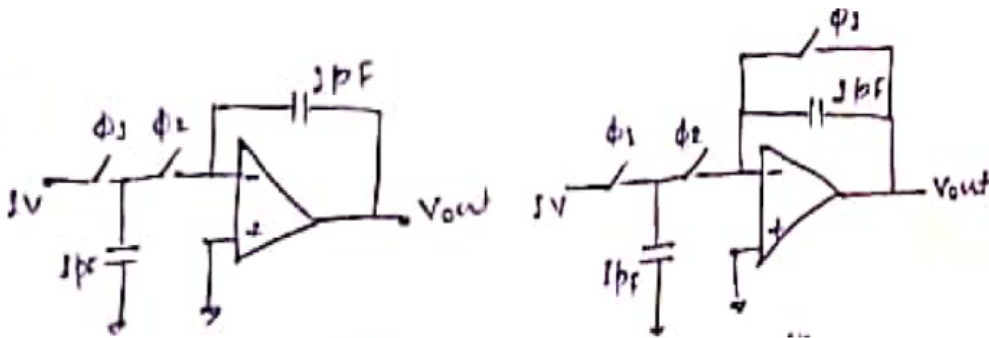
1. Plot V_x during the initial pulses and after many pulses for the following cases: (i) $C_1 = C_2$
(ii) $C_1 \neq C_2$



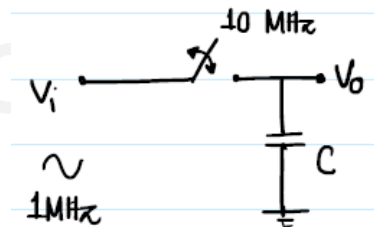
2. Find the steady-state value of V_{out} . The inputs are 1.8 V and 1 V. The value of all capacitors is $C = 1 \text{ pF}$. ϕ_1 and ϕ_2 are non-overlapping clocks.



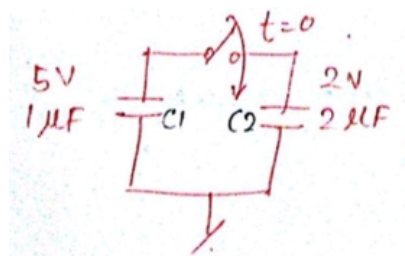
3. The input is 1 V. The value of all capacitors is $C = 1$ pF. Plot V_{out} for more than two cycles of the non-overlapping clocks ϕ_1 and ϕ_2 .



4. The switch is non-ideal (finite resistance, non-linear).
 (a) Determine the frequency content in V_o .
 (b) Which frequencies are dominant?

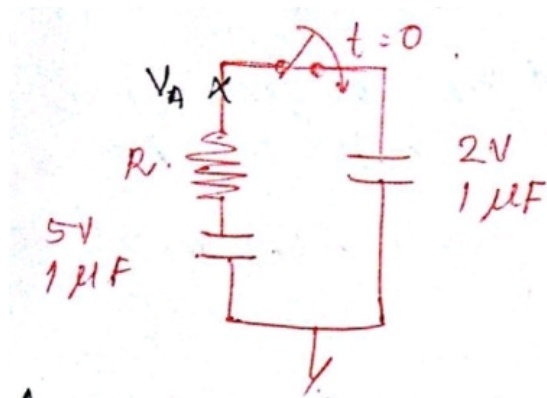


5. (a) Capacitors C_1 and C_2 are initially charged to 5 V and 2 V, respectively. The switch is closed at $t = 0$. Comment on the final voltage.

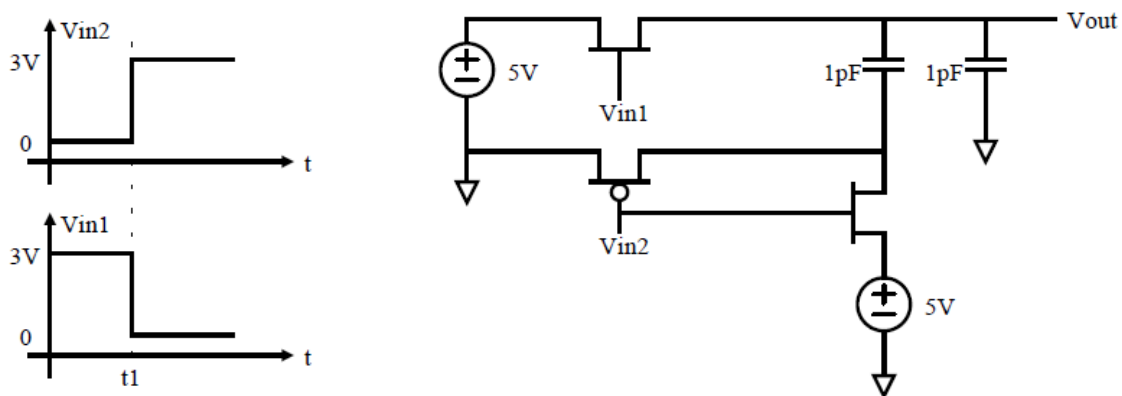


- (b) A resistor R is introduced into the circuit shown in the figure.
 i. What will be the voltage V_A ?

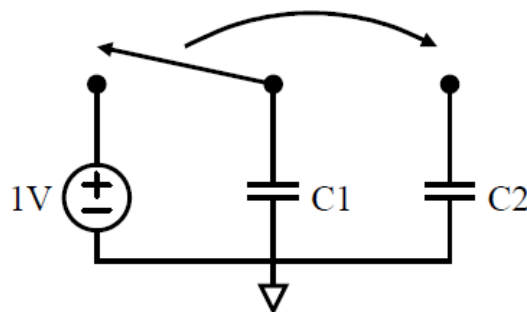
- ii. Can this be represented using mathematical equations?
- iii. What will be the equation of the current?



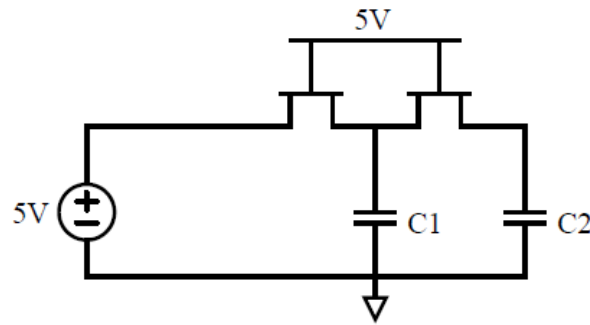
- (c) Is energy conserved in case (a)? Explain. If not, where did the remaining energy go?
 - (d) Is energy conserved in case (b)? Explain.
6. Plot V_{out} with respect to the given input waveforms.



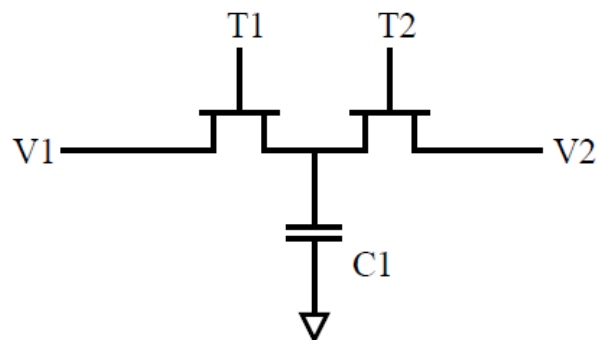
7. For the following circuit, at time $t = 0$, the switch transitions from position A to position B. Determine and sketch the voltage waveform observed at node B.



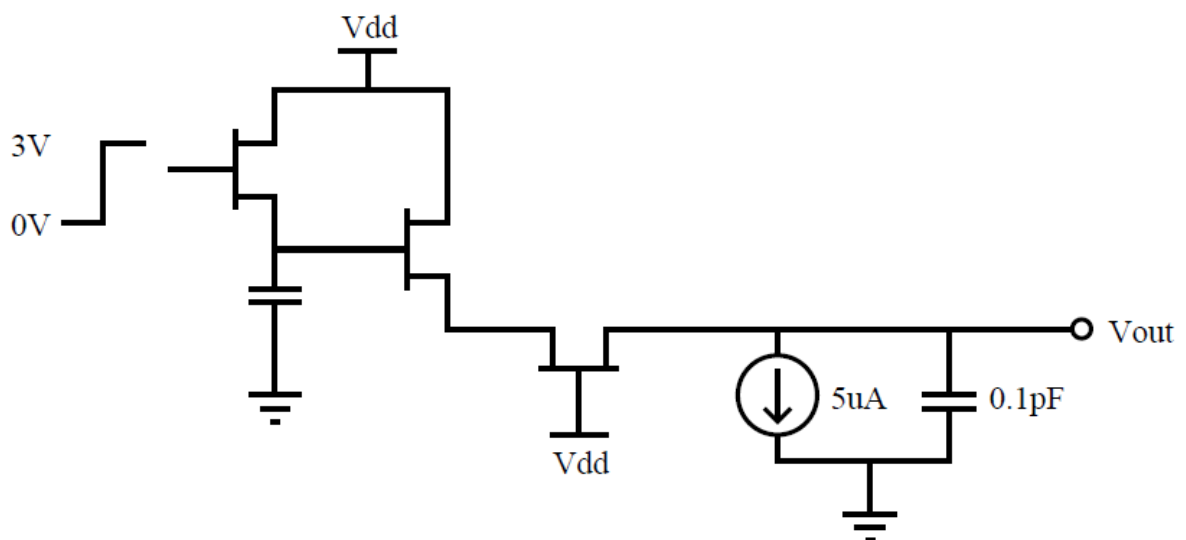
8. For the following circuit, determine the voltage values at nodes A and B. Assume the threshold voltage V_T of the transistor is 1 V.



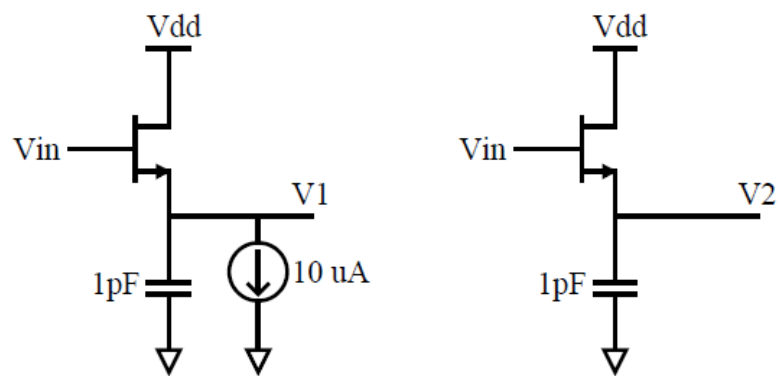
9. In the following circuit, a capacitor is connected between two ideal MOS switches, T_1 and T_2 , which are alternately turned on at a frequency f_c . Determine the average current flowing from node 1 to node 2. Additionally, calculate the equivalent impedance seen from node 1 to node 2.



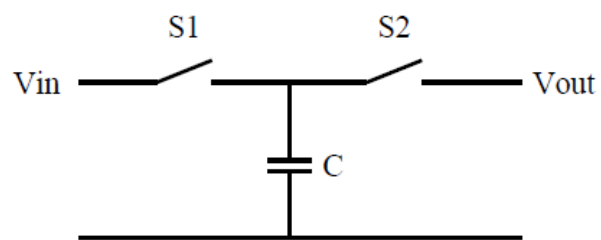
10. Calculate the output voltage after 5 s based on the initial conditions and circuit parameters.

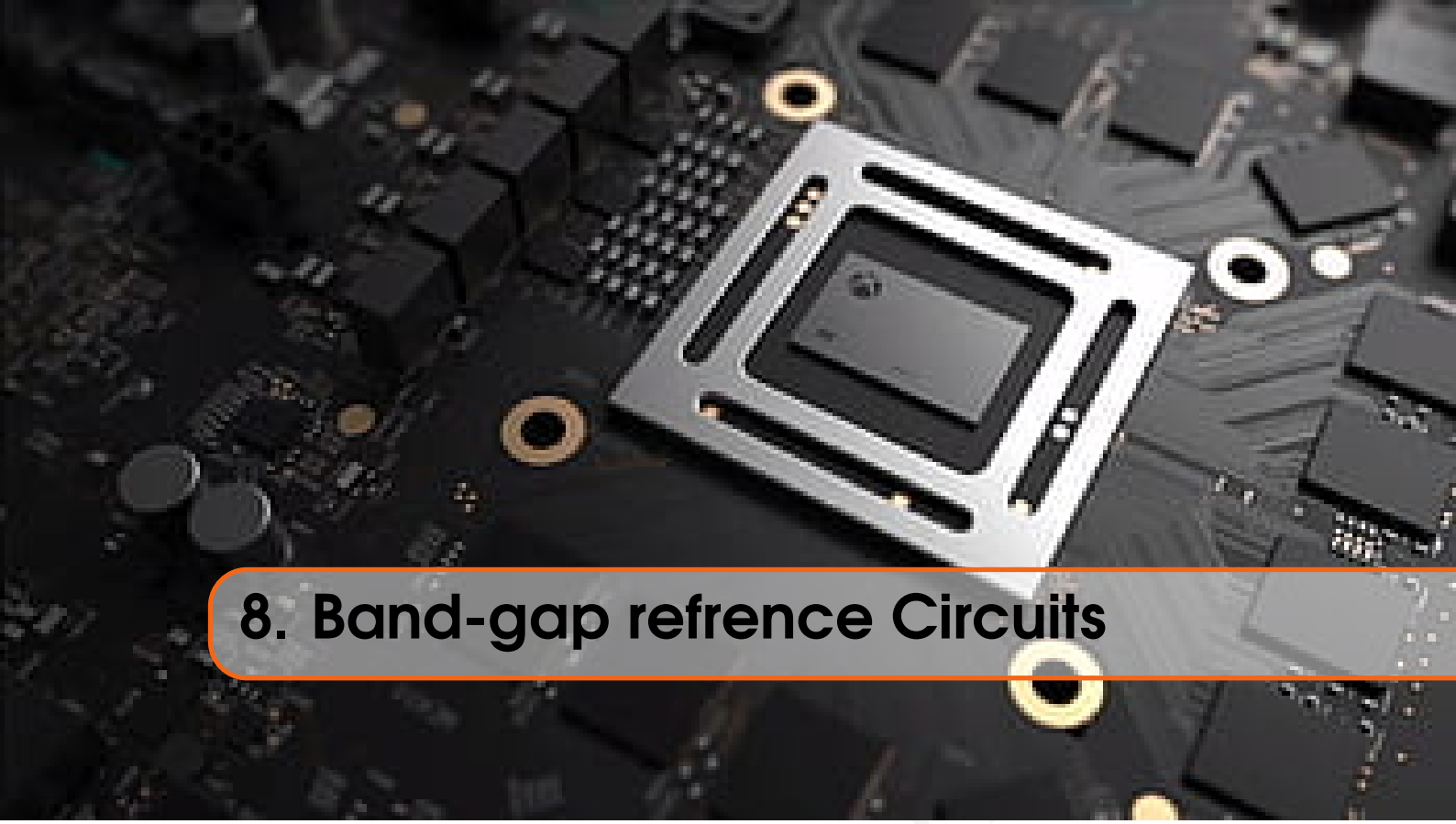


11. Initially, $V_1 = V_2 = 1$ V and $V_{in} = 0.7$ V. If V_{in} changes to 1.5 V, determine the final states of the circuit.



12. What is the equivalent value of resistance.



A close-up photograph of a microchip mounted on a dark printed circuit board (PCB). The chip is square with a central square area and is surrounded by numerous gold-colored pins. The PCB is populated with various other components, including smaller chips and resistors.

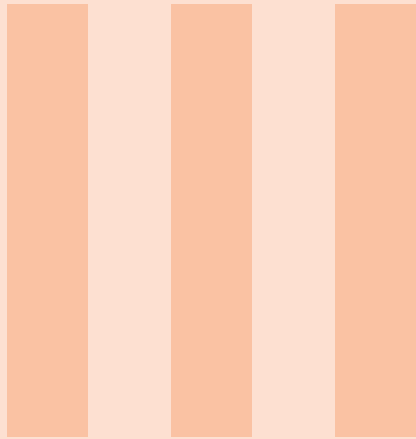
8. Band-gap reference Circuits

8.1 Prerequisites

Bandgap circuit design in CMOS process by Analog Snippets

8.2 Questions

1.
 - a) Draw a BGR (Bandgap Reference) circuit. Explain the op-amp's role and sign convention.
 - b) Can we use MOSFETs instead of PNP transistors?
 - c) What happens if the resistors used have temperature dependency? How do you deal with it?
 - d) How do you ensure stability in a BGR circuit?



Miscellaneous

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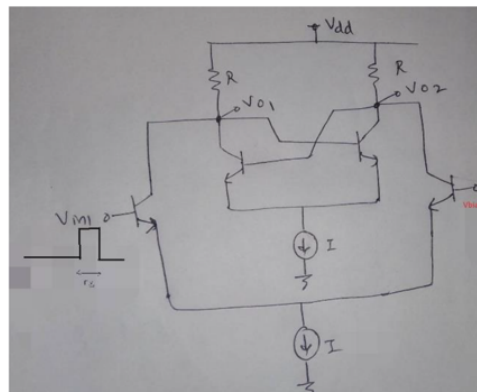
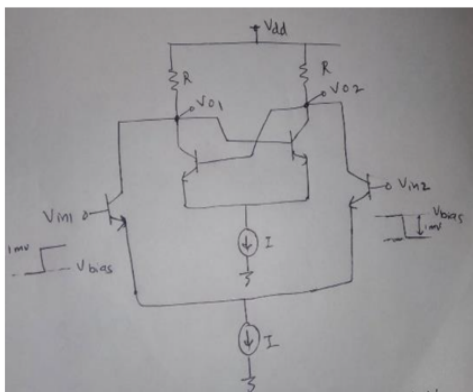
9. Miscellaneous

9.1 Questions

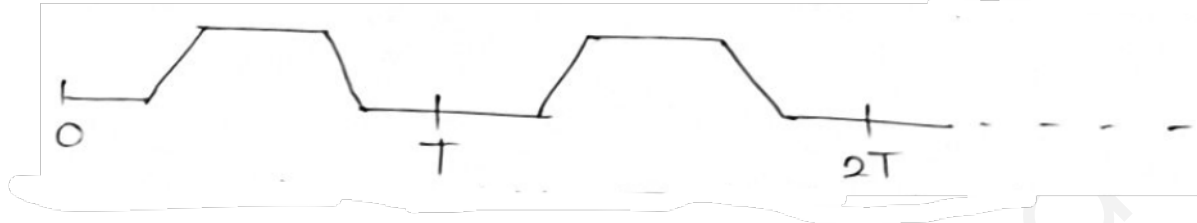
1. Draw both PMOS and NMOS current mirrors. Determine the voltage at each node separately. Then, connect the two circuits such that there are no floating nodes. Finally, find the voltage at the intersection point.
2. Find V_{out} .



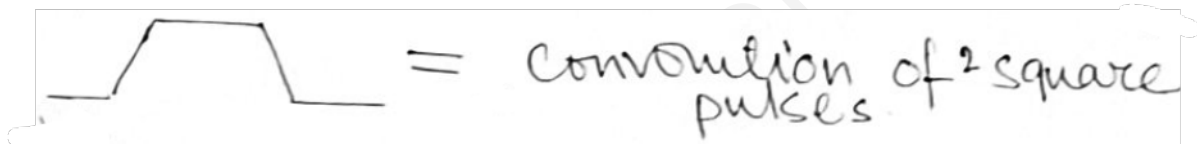
3. Draw V_{O1} and V_{O2} for
 - (a) the differential input shown in the figure, and
 - (b) a pulse input of 1 ms duration, assuming the transistors are biased.



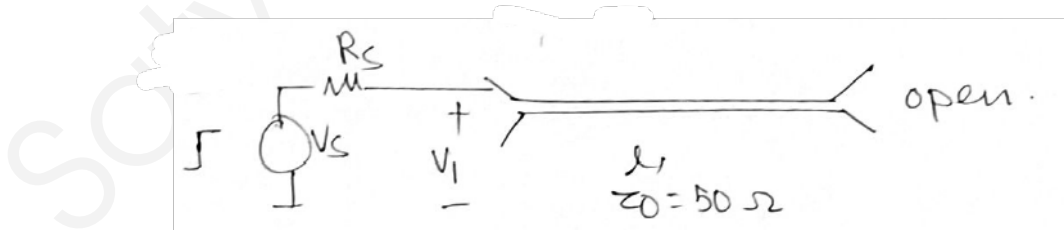
4. You are given a train of pulses having a certain rise time and fall time.



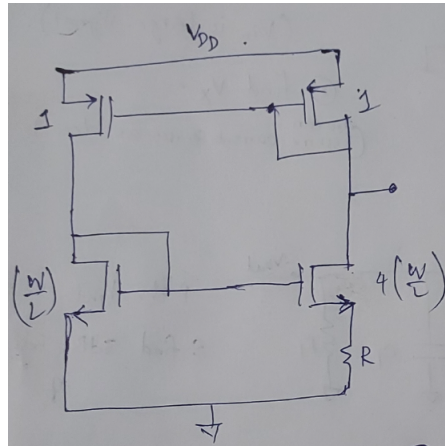
How would you model the pulse train in the frequency domain and time domain to obtain its Laplace Transform? **Hint:**



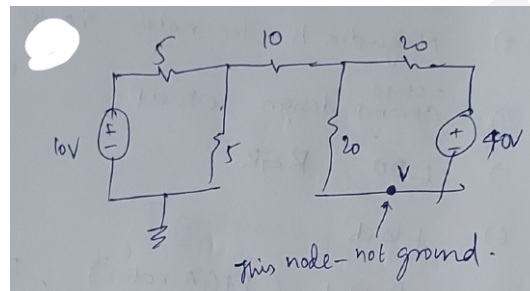
5. For a cascode of two amplifiers with gains A_1 and A_2 , noise figures NF_1 and NF_2 , and input third-order intercept points $IIP3_1$ and $IIP3_2$, what will be the overall noise figure and $IIP3$ of the system? (Question for RFIC profile.)
6. The line is matched to R_s . The input is a 1 V step.
- Find V_1 .
 - Model the line assuming it is lossless, and verify V_1 using this model.



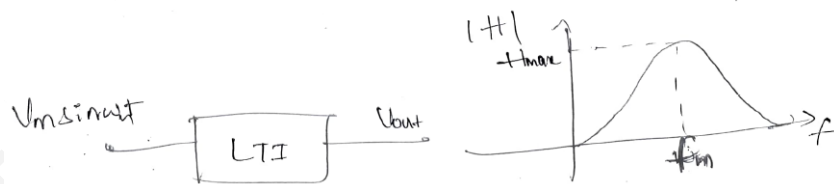
7. (a) Determine the type of feedback present in the circuit, identify where to break the loop to analyze the feedback, and specify what should be checked before breaking any loop.
- (b) What are the currents through all transistors? Derive the loop gain expression. (Note: Drawing the small-signal circuit is not allowed.)
- (c) What is the condition for the circuit to exhibit positive feedback?



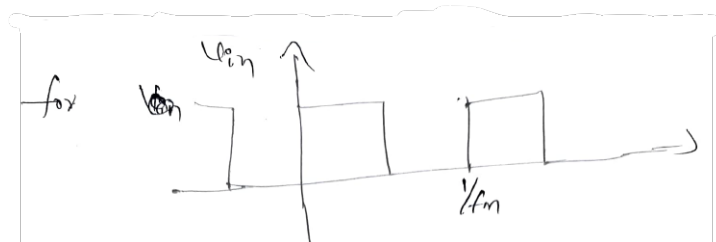
8. Find V . (You are not allowed to use nodal analysis. You should answer without lengthy math.)



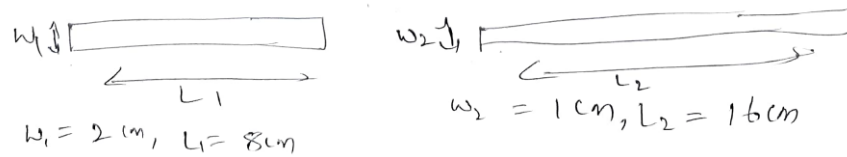
9. (a) Draw V_{out} for an input $V_m \sin(\omega_m t)$ in an LTI system with its characteristics shown below.



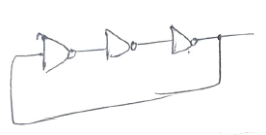
- (b) Draw V_{out} for the input shown below.



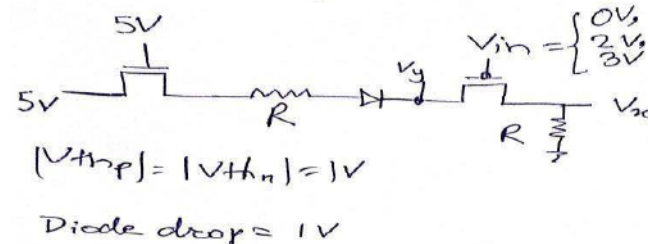
10. (a) Calculate the resistance ratios of both metals.
(b) Calculate the ratio of capacitances of both metals.



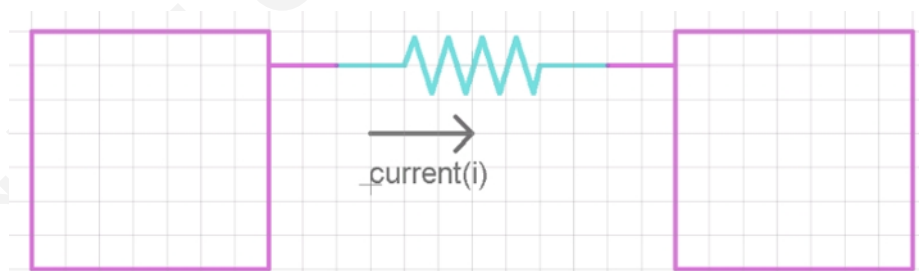
11. (a) Draw V_{out} and explain the working of the circuit.



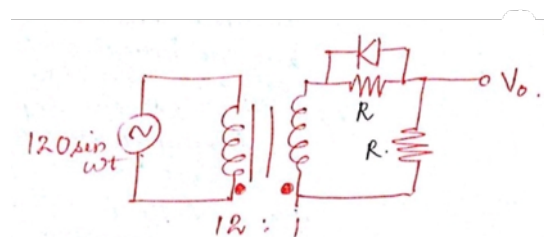
- (b) What is the gain of the inverters at $t = 0$ and at steady state?
 (c) In which region will they operate at $t = 0$ and at $t = \infty$?
 12. Find V_X and V_Y for the given different values of V_{in} shown in the figure.



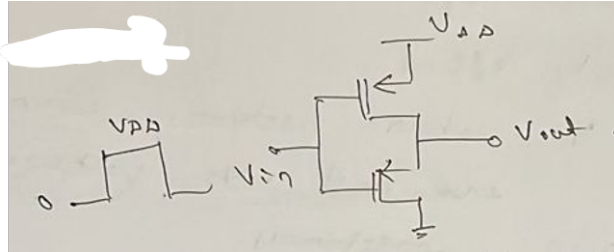
13. Two black boxes are given, each containing an unknown network of resistors along with current and voltage sources. One wire comes out of each of the two black boxes, as shown. If we connect a resistor between these wires, can we say anything about the current through it?



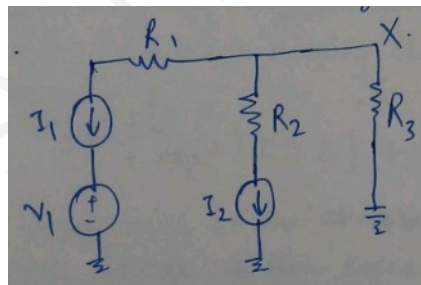
14. An AC source is given by $120 \sin \omega t$, and the transformer has a turns ratio of 12:1. The diode is ideal. Comment on V_o and plot it.



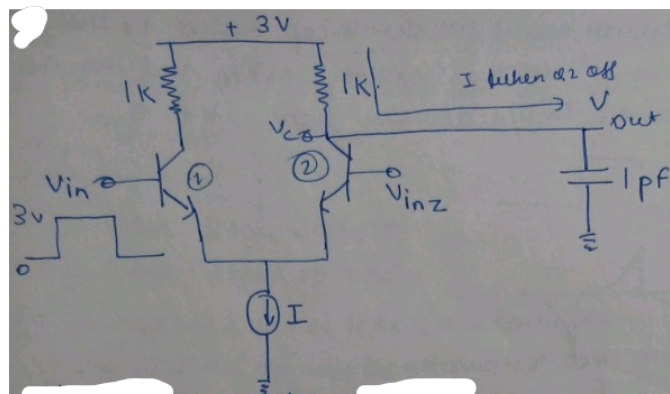
15. (a) Draw a CMOS inverter. Plot the input and output characteristics for a pulse input with minimum = 0 V and maximum = V_{DD} .
 (b) What happens if both transistors are PMOS?



- (c) What happens if both transistors are NMOS? (Answer: Buffer)
16. a) Draw the cross-section of an NMOS transistor.
 b) What is inversion?
 c) Explain the body effect when the body is connected to positive and negative voltages.
 d) Represent the MOS capacitances.
17. Discuss the Voltage Transfer Characteristic (VTC) of an inverter. How does the VTC change with increased sizing of NMOS and PMOS transistors?
18. What is the stability criterion for a system when the loop gain is 1 and the loop phase angle is 150° ? Comment on the system's stability.
19. Calculate the voltage at node V_X . Discuss whether the components V_1 , R_1 , and R_2 have any impact on the value of V_X .



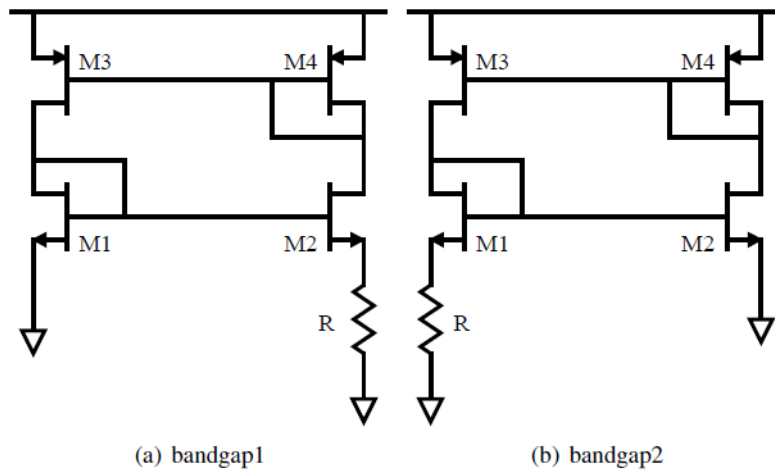
20. Given that V_{in2} is the complement of V_{in} , determine the time at which V_{out} reaches 2.9 V.



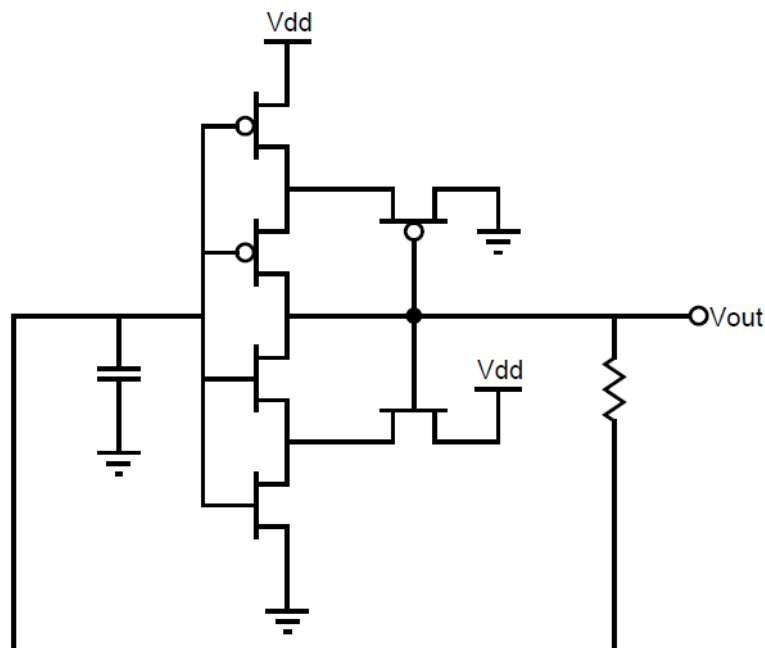
21. You are probing a square wave pulse in the laboratory with a rise time of 5 ns and a fall time of 2 ns. Determine the minimum bandwidth required for the oscilloscope to accurately observe the signal.

(Answer: The time it takes for an RC circuit to transition from 10% to 90% of its final value is given by $t = \ln(9) \cdot RC$. To capture the signal's fall time of 2 ns, the oscilloscope bandwidth must be greater than $BW = \frac{\ln(9)}{2\pi \cdot 2 \text{ ns}} \approx 174 \text{ MHz}$. A suitable choice is an oscilloscope with a bandwidth of at least 200 MHz. To minimize measurement error, it is recommended to use an oscilloscope with a bandwidth approximately three times higher, i.e., 600 MHz.)

22. Compare the functionality of the following two circuits. How do they differ in operation, and which one provides a more stable or accurate reference?

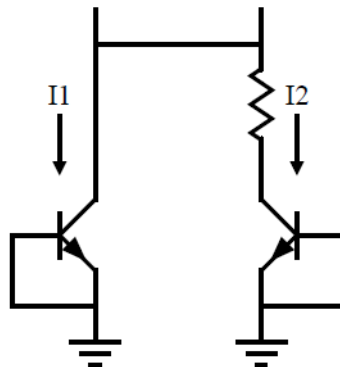


23. Draw the output waveform corresponding to the given circuit .

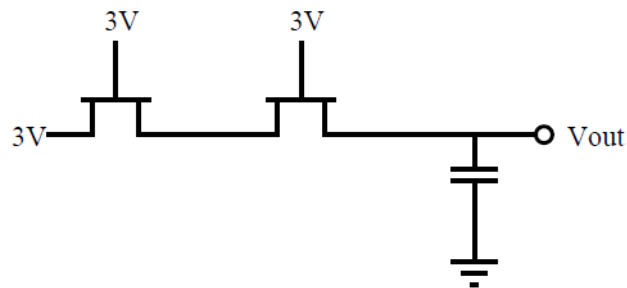


24. Describe how I_1 and I_2 vary with temperature. Explain the underlying physical or circuit

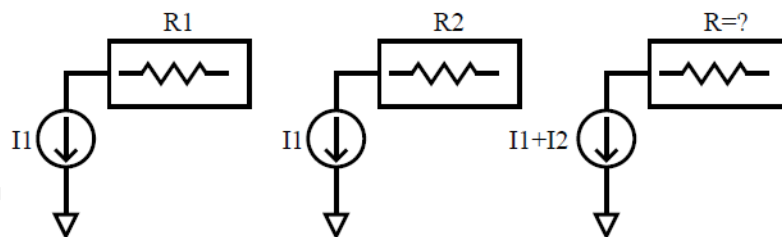
mechanisms affecting their temperature dependence.

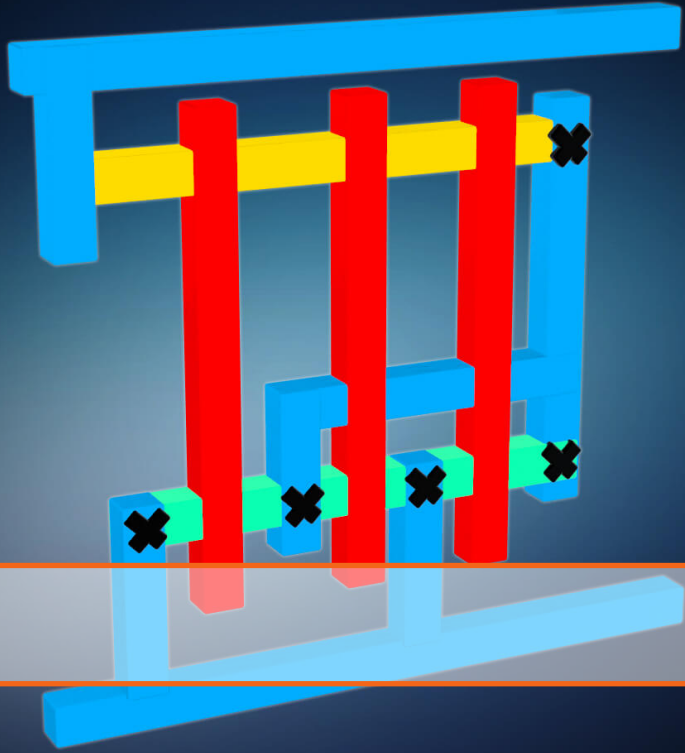


25. Determine the output voltage of the circuit based on the given conditions.



26. Calculate the value of R . Assume the network is entirely resistive.





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